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A 0.5-V SUBTHRESHOLD-LEAKAGE SUPPRESSED FULLY DIFFERENTIAL CMOS SWITCHED-CAPACITOR AMPLIFIER WITHOUT TRANSMISSION GATES

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ABSTRACT

This paper presents a 0.5-V subthreshold-leakage suppressed fully differential CMOS switched-capacitor amplifier with an analog T-switch, without transmission gates. The circuit design and major properties of the circuit are covered and the experimental results demonstrate the performance of this circuit. The switched-capacitor amplifier operates with a signal-to-total harmonic distortion ratio of 37dB for a 10-kHz sinusoidal amplitude input of 0.1Vpp. The power dissipation of this circuit is 36.21-μW. The circuit was fabricated using a standard 0.18-μm CMOS process. Experimental results confirmed the applicability of using analog T-switches to fulfill the circuit requirements.

Keywords: low-voltage, subthreshold-leakage, CMOS, switched-capacitor amplifier.

1. INTRODUCTION

Analog signal amplification in a sampled-data system can be performed by switched-capacitor (SC) amplifiers (Martin *et al*. 1987). SC amplifiers are already widely used in the design of digital-to-analog converters (Yang and Martin 1989). The schematics for an SC amplifier is shown in Fig. 1. The phase signals ϕ_1 (ϕ_1') and ϕ_2 (ϕ_2') are non- overlapping. ϕ_1' (ϕ_2') is slightly more advanced than ϕ_1 (ϕ_2). Assuming an infinite operational amplifier (op amp) gain, the output voltage at the end of ϕ_2 is given by

$$V_{out}(nT) = \frac{C_1}{C_2} V_{in}\left(nT - \frac{T}{2}\right) \tag{1}$$

irrespective of the op amp offset voltage. If the clock waveforms (shown in parentheses) are used, then an inverting function of the following form is realized

$$V_{out}(nT) = -\frac{C_1}{C_2} V_{in}(nT) \tag{2}$$

is independent of the op amp input offset voltage. During the reset phase (ϕ_1), C_3 is connected in a feedback around the op amp which causes the output to change only by the op amp input offset voltage. The switches are realized as complementary metal oxide semi-conductor (CMOS) transmission gates. For low supply voltages, a conductance gap begins to appear around the middle of the supply range (Crols and Steyaert 1994). This means that under low-voltage operation, this configuration no longer works. Several low-voltage SC amplifiers have been reported, but all are implemented in a high-threshold voltage (high-V_{th}) process (Yoshizawa *et al*. 1999; Lee and Lu 2010). Previous works mainly tackled the realization of low-voltage analog circuits using high-V_{th} devices, and consequently the issue in charge-based analog circuits was high resistance of metal oxide semi-conductor (MOS) switches. To reduce on-state resistance, gates of MOS switches are widened or higher voltages are applied by bootstrap (Ishida *et al*. 2006).

While moving into ultra-deep submicron CMOS technologies, the threshold is reduced as the supply voltage is decreased. In the low-V_{th} process, however, nonlinear subthreshold leakage current can be a critical issue for analog circuits. There are two ways of reducing the leakage current without significantly increasing the length of a transistor, which would unacceptably increase the on-resistance of the switch (Ishida *et al*. 2006; Roh *et al*. 2009). The authors have presented a 0.6-V subthreshold-leakage suppressed fully differential CMOS SC amplifier (Lee and Lu 2013) based on an analog T-switch (AT-switch)

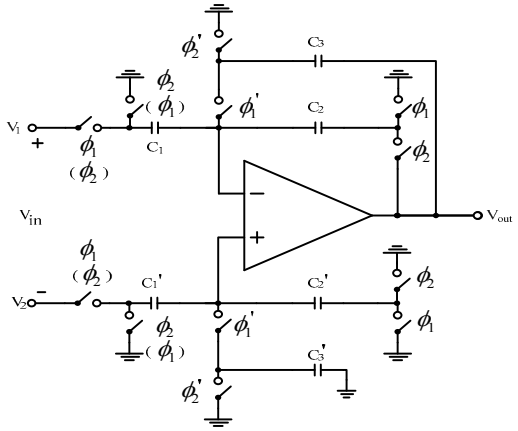

Fig. 1 A differential-to-single-ended CMOS SC amplifier. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).

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scheme (Ishida *et al*. 2006). The results of this SC amplifier exhibit subthreshold leakage current improvement, however, which still exists because of the use of the CMOS transmission gates in the common-mode feedback (CMFB) circuit for the op amp.

This paper describes the design of a 0.5-V subthreshold-leakage suppressed fully differential CMOS SC amplifier in standard 0.18μm CMOS technology, using an AT-switch scheme without CMOS transmission gates. In section 2, the circuit schematics and theoretical background of this SC amplifier are established. Experimental results are presented in section 3 to support the proposed ideas. The conclusion follows in section 4.

2. CIRCUIT DESCRIPTION

Figure 2 shows the low-voltage subthreshold-leakage suppressed fully differential CMOS SC amplifier without transmission gates, where switches S1_AT and S4_AT (S1'_AT and S4'_AT) are AT-switches, switches S2_S and S3_S (S2'_S and S3'_S) are stack switches, and switches S5-S6 (S5'-S6') are nMOS transistors. The description of each AT-switch and stack switch is given in Fig. 3. In order to use the AT-switch, an analog reference voltage is used: common-mode voltage $V_{cm} = -0.12$V at the op amp input, the op amp output, and the circuit input, in order to maximize the signal swing. The principle of the subthreshold leakage suppression scheme is similar to that presented in (Lee and Lu 2013). An extra pair of small matched capacitors C_{dg} and C'_{dg} (denoted by dashed lines) shown in Fig. 4 are included as optional deglitching capacitors (Matsumoto and Watanabe 1987). These capacitors are used to provide continuous time feedback during the non-overlapping times when all the switches are open, and will thus eliminate the potential generation of output glitches.

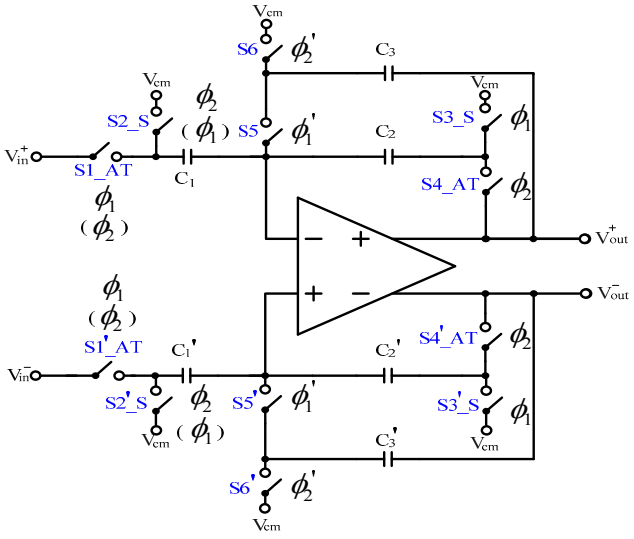

Fig. 2 Low-voltage subthreshold-leakage suppressed fully differential CMOS SC amplifier without transmission gates. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).

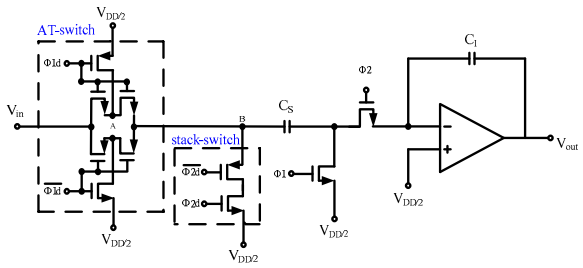

Fig. 3 AT-switch and stack switch in an SC integrator (Ishida *et al*. 2006).

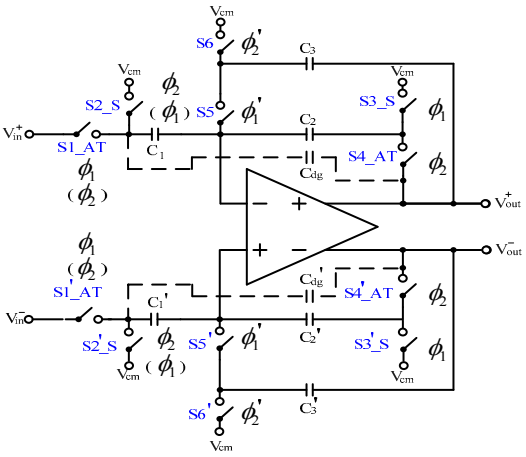

Fig. 4 Low-voltage subthreshold-leakage suppressed fully-differential CMOS SC amplifier without transmission gates and with matched deglitching capacitors C_{dg} and C'_{dg} to eliminate the generation of output glitches during the non-overlapping times of the clock phases.

Figure 5 shows the op amp that is used. It is based on a folded-cascode fully differential p-type two-stage Miller-compensated configuration. The second stage is a common-source gain stage with active load that allows a large output swing. In order to avoid the CMFB circuit for the first stage, transistors *M51*, *M52*, *M61*, and *M62* similar to those presented in (Waltari and Halonen 1998) are used. For the second stage, *M10, M12*, *RCM+*, and *RCM−* act as the common-mode feedback loop. The common-mode signal detector is realized with *RCM+* and *RCM−* without CMOS transmission gates. The results of simulations predicting the performance of the op amp with a load of 6-pF are summarized in Table 1. The unity-gain bandwidth of the op amp is simulated to be 12.4-MHz with a phase margin of 80°. The capacitors used in the switched- capacitor amplifier are MIM (metal-insulator-metal) capacitors.

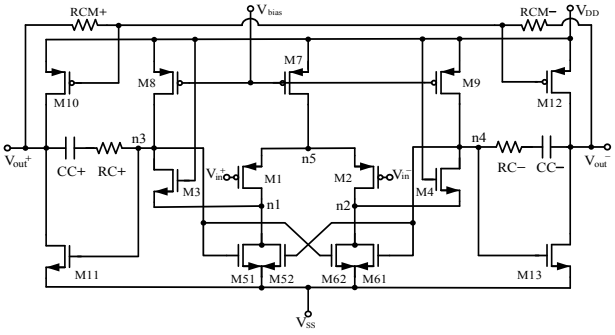

Fig. 5 Low-voltage op amp

Table 1 Simulated op amp performance

Power supply voltage	± 0.25-V
Unity-gain bandwidth	12.4-MHz
Phase margin	80°
DC gain	60.4dB
Input offset voltage	62.3-mV
Output swing	-0.188-V ~ 0.247-V
Power consumption	30.1-μW

3. EXPERIMENTAL RESULTS

Based on the principles presented in sections 1 and 2, a draft design for a 0.5-V subthreshold-leakage suppressed fully differential CMOS SC amplifier without transmission gates has been established. This SC amplifier was operated with ±0.25-V. The capacitor sizes used were $C_1(C_1')$ = 1.25-pF, $C_2(C_2')$ = 0.25-pF, and $C_3(C_3')$ = 0.75-pF, for a nominal gain of -5. The circuit shown in Fig. 4 was fabricated using TSMC 0.18-μm CMOS technology. The threshold voltages were 0.269-V and −0.127-V for the medium-V_{th} nMOS transistors and pMOS transistors, respectively.

The measured input/output waveforms for a 0.1-V peak-to-peak, sinusoidal differential input signal were recorded, and are presented in Fig. 6. To obtain a satisfactory settling behavior under a 12.4-MHz unity-gain bandwidth of the op amp, the clock frequency was set at 1-MHz and the input signal was set to 10-kHz. It can be seen that the gain was very close to the nominal value of -5. Shown in Fig. 7 are the simulated input/output waveforms of the SC amplifier in (Lee and Lu 2013) for a 0.12-V peak-to-peak sinusoidal differential input signal.

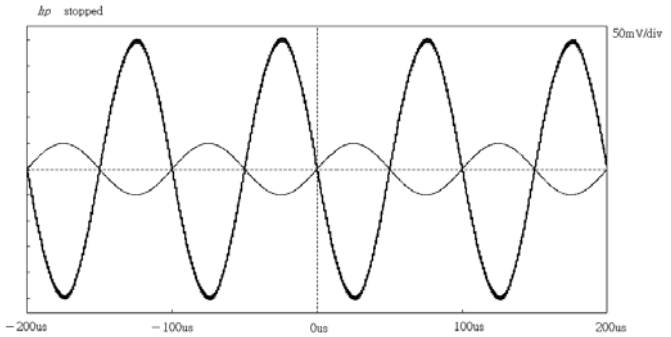

Fig. 6 Measured differential input and output waveforms of the Fig. 4 circuit (f_{clk} = 1-MHz, f_{in} = 10-kHz, sinusoidal differential input voltage = 0.1-V_{pp})

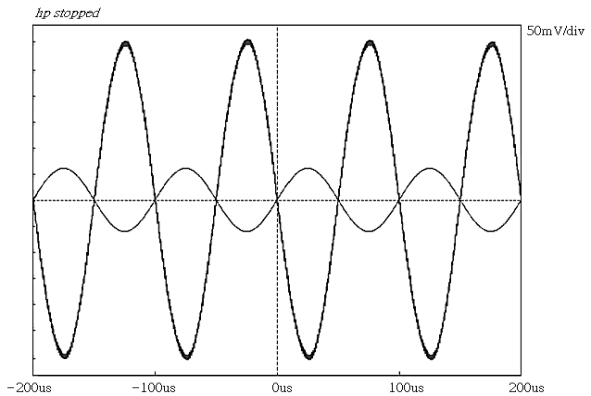

Fig. 7 Measured differential input and output waveforms of the SC amplifier in (Lee and Lu 2013) (f_{clk} = 1-MHz, f_{in} = 10-kHz, sinusoidal differential input voltage = 0.12- V_{pp})

Figures 8 and 9 show the resulting output spectrum. As shown in Figs. 8 and 9, the even-order harmonics have been largely attenuated by the fully differential topology. The largest harmonic components were at 38 -dB, and at 38 -dB below the fundamental of the input signal, respectively. The signal-to-THD (total harmonic distortion) ratios were 37 -dB and 36 -dB, respectively. The circuit in Fig. 4 dissipates 36.21-μW when using a 0.5-V power supply. The experimental results of the proposed SC amplifier are summarized in Table 2 and compared to other existing CMOS SC amplifiers. In the design proposed in this paper, the operating supply voltage is lower than those of reported by (Yoshizawa *et al*. 1999; Lee and Lu 2010; Lee and Lu 2013). The signal-to-THD ratio is higher than that found in (Martin *et al*. 1987) and lower than those reported by (Yoshizawa et al. 1999; Lee and Lu, 2010), principally because of the lower supply voltage. The proposed subthreshold-leakage suppressed SC amplifier without CMOS transmission gates achieves higher signal-to-THD ratio than that of the switched-capacitor amplifier in (Lee and Lu 2013), this is due to the leakage current that introduces nonlinear errors. A die photograph of the subthreshold-leakage suppressed SC amplifier without CMOS transmission gates is shown in Fig. 10.

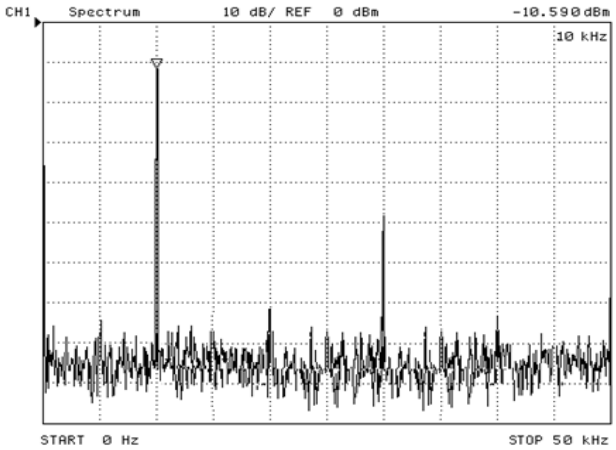

Fig. 8 Measured output spectrum of the Fig. 4 circuit

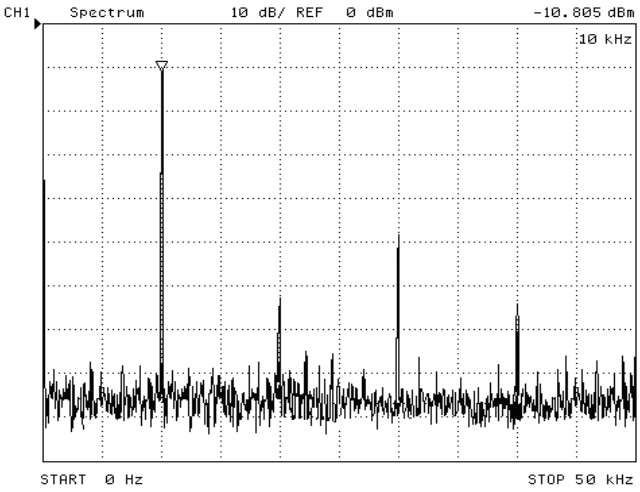

Fig. 9 Measured output spectrum of the SC amplifier from (Lee and Lu 2013).

Table 2 Summary and comparison of known CMOS SC amplifier performance

Design	Reference (Martin, Ozcolak, Lee, and Temes, 1987)	Reference (Yoshizawa, Huang, Ferguson, and Temes, 1999)	Fig. 2 of reference (Lee and Lu, 2010)	Fig. 5 of reference (Lee and Lu, 2010)	Reference (Lee and Lu, 2013)	Fig. 4 of this design
Technology	3-μm CMOS	1.2-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Topology	differential-to-sing-le-ended	fully differenti-al	fully differenti-al	fully differenti-al	fully differenti-al	fully differenti-al
Clock frequency	1-MHz	16-kHz	1-MHz	1-MHz	1-MHz	1-MHz
Signal-to-THD ratio	30dB@10-kHz	69dB@1-kHz	57dB@10-kHz	50dB@10-kHz	36dB@10-kHz	37dB@10-kHz
Supply voltage	unknown	± 2.5-V	± 0.5-V	± 0.5-V	± 0.3-V	± 0.25-V
Power consumption	unknown	unknown	206.5 -μW	206.6-μW	142.92-μW	36.21-μW

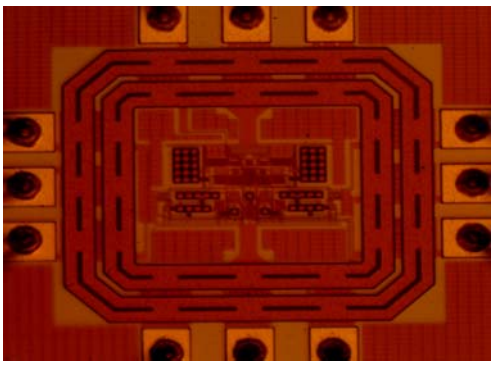

Fig. 10 Die photograph of the subthreshold-leakage suppressed SC amplifier without CMOS transmission gates.

4. CONCLUSION

A 0.5-V subthreshold-leakage suppressed fully differential CMOS SC amplifier without transmission gates has been described. The AT-switch scheme was used in this circuit. The SC amplifier achieves 37 dB of signal-to-THD ratio, for an input 10kHz sinusoidal amplitude of 0.1Vpp and consumes 36.21-μW. The whole circuit was fabricated using a standard 0.18μm CMOS process. The circuit was designed, fabricated and all aspects of its performance were examined and confirmed. The proposed circuit represents an advance in the design of ultra-low-voltage SC amplifier.

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