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Bidirectional Interleaved Flyback Converter for DC Microgrid System Applications

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ABSTRACT

A bidirectional flyback converter was devised, built and tested. Such a device would be useful as part of a larger DC microgrid system that may be installed as part of a residential energy storage solution. Two bidirectional flyback converters were connected in parallel with an interleaved duty cycle control to decrease ripple currents on the input voltage and output load. When energy storage units such as batteries are charged from the DC bus, the flyback delivers power from the DC microgrid to either the load or storage side. When the energy of the energy storage unit is released, the flyback mechanism reverses the power flow and releases the stored energy back through the DC microgrid. The principle benefit of such a device is the relative simplicity of the circuit, and fewer powered devices. No fast recovery diode is used in this design, improving efficiency. The operational principles, system characteristics, design example and control characteristics are provided in detail. A hardware circuit with a 190 V input and 48 V/8.33 A output was constructed. The feasibility of the tested device was substantiated by the test results and waveform outputs.

Keywords: Flyback, DC microgrid system, interleaved PWM converter.

1. INTRODUCTION

Renewable energy sources have been widely developed to reduce the industrial burden placed on of fossil fuels and the global warming effect they produce. However, renewable energies such as wind and solar power still require much development before widespread deployment can occur. In order to integrate renewable energy sources into a common voltage bus, techniques have been developed to convert the different kinds of voltage sources into direct current (DC). DC microgrid systems are used to integrate different utility systems found in wind power, PV power, storage systems, residential houses, commercial buildings and industry, into a common DC bus. Energy storage units are fundamental to maintaining stable DC bus voltage as the voltages generated by renewable sources may be either too great or too little under different conditions. If sufficient renewable energy is generated, redundant energy can be stored in energy storage units, and when the voltage level is insufficient, or there are power outages, that stored energy can then be released back into the system to provide extra load. To realize these functions effectively, bidirectional DC to DC converters are often used in the form of a DC microgrid system, which is paired with battery banks or super capacitors. Isolated DC to DC converters with bidirectional power flow capabilities were initially researched and proposed for energy storage applications, including most prominently, electric vehicle systems. Half-bridge (dual) topologies and full-bridge (dual) topologies with symmetric circuits on both voltage sides are normally selected to achieve bidirectional power flow. The pulse-width modulation control and frequency control are usually selected to generate the necessary gating signals for all powered devices. To eliminate switching losses on active devices, soft-switching approaches have been developed over the course of several years. Among these techniques there are active-clamping (Chen *et al*. 2000), phase-shift pulse-width modulation (Poshtkouhi and Trescases 2015; Xu *et al*. 2004; Garcia *et al*. 2005; Yamamoto *et al*. 2006; Chu and Chen 2009; Wu *et al*. 2010) and resonant frequency control (Jiang *et al*. 2015), which are often adopted in commercial integrated circuits (IC). However, the main problems with these circuit topologies are that there are too many powered devices that increases production costs. A greater number of powered devices in a circuit will also decrease circuit reliability. For lower power rated energy storage units in residential buildings, bidirectional power converters with a simple circuit structure and low costs could replace the complicated circuit topologies that may currently form a research engineer's area of interest.

In this paper, a bidirectional interleaved flyback converter is planned, produced and tested. The main advantages of the approach in this paper are the simple circuit structure, lower cost, fewer onboard powered devices and fewer ripple currents on both the input and output sides. Two parallel flyback converters are operated with an interleaved duty-cycle control so that the input and output currents of the two flybacks are interleaved with a one-half switching cycle. The ripple current frequency is two times that of the switching frequency, decreasing the output capacitance. Either power switch can be used as a main switch to control output voltage or the synchronous rectifier to reduce conduction losses. The circuit presented for readers is based on a lower power model that operates under a 400 W output power load.

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2. PROPOSED CONVERTER

The basic schematic blocks of a DC microgrid with a bipolar voltage system are demonstrated in Fig. 1 AC to DC bidirectional converters are conventionally placed between AC utility and DC microgrid systems to provide power, or absorb power, when the DC bus voltage on the DC microgrid system is lower or higher than the desired voltage value. Clean energy sources through power converters can be converted to a stable DC voltage by use of DC microgrid systems. Energy storage units (ESUs) such as battery banks or super capacitors are normally connected to DC microgrid systems by a powered bidirectional electronic circuit. To increase system reliability DC microgrid systems can use the bipolar voltage levels +190V, –190V and 0V, in place of the unipolar voltage levels, +380V and 0V, which prevents abnormal conditions. If a fault occurs in a bipolar voltage system, DC power is still supplied from the DC microgrid by the other two wire connections. Therefore, the DC microgird bipolar voltage system shows improved reliability in during faults. Bipolar voltage systems can also be used to provide a +380V voltage level to industry loads and a +190V or –190V voltage level to residential homes. Normally, voltage balancing converters are required to avoid unbalanced voltage loads in bipolar systems. The bidirectional DC to DC converter developed here is focused on a powered, scaled-down circuit for ESUs that could be used in future residential homes.

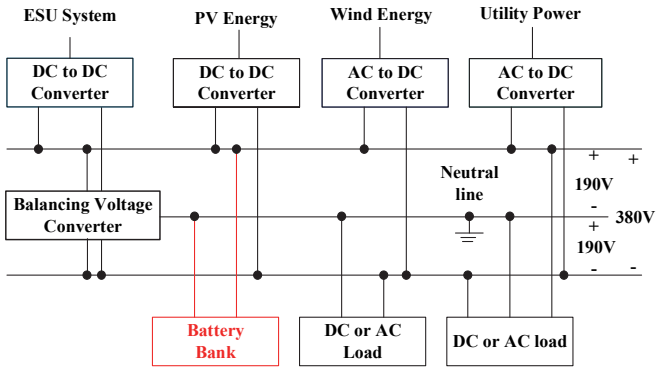


Fig. 1 Schematic block diagram of a generic bipolar voltage DC microgrid system.

Figure 2 shows the circuit diagram of the interleaved bidirectional flyback system used in this paper. When the flyback is operated as a battery charger, the 190 V input voltage from the DC microgrid is converted to a 48 V output for a battery bank. The proposed converter includes two bidirectional flyback converters connected in parallel with interleaved PWM operation. MOSFETs S_1 and S_2 function as the primary power switches and the PWM signals are phase-shifted by $T_{sw}/2$. MOSFETs S_3 and S_4 function as synchronous rectifiers to decrease reduce power losses. T_1 and T_2 are the isolated transformers that provide galvanic isolation. T_1 and T_2 can store energy on the magnetizing inductors when S_1 and S_2 conduct. The voltage stresses of S_1 and S_2 are related to V_{in}, V_o, turn-ratio n, leakage inductances of T_1 and T_2, and the parasitic capacitance and the output capacitances of S_1 and S_2. Each flyback provides $P_o/2$ to the load side. The driving signals from S_1 and S_2 are based on the interleaved PWM operation. On the other hand, MOSFETs S_1 and S_2 operate as synchronous rectifiers and the MOSFETs S_3 and S_4 function as active switches with the interleaved PWM operation to realize the reverse power flow. Since the adopted converter is symmetrical in operation for both directions of power, only forward power flow operation will be discussed further in this paper. The main voltage and current waveforms under continuous conduction mode (CCM) are shown in Fig. 3. The circuit tested in this paper was operated under the following conditions: (1) circuit is operated under CCM, (2) $S_1 \sim S_4$ are ideal, (3) $L_{r1} = L_{r2}$ and $L_{m1} = L_{m2}$, and (4) $n_1 = n_2 = n_p/n_s$. The duty cycles of S_1 and S_2 are $d < 0.5$ and the duty cycles of S_3 and S_4 are $1 - d$. Fig. 4 illustrates the topological circuits corresponding to each operational stage of the converter. Due to the conditions of $S_1 \sim S_4$, six topological stages can be found in a complete switching cycle.

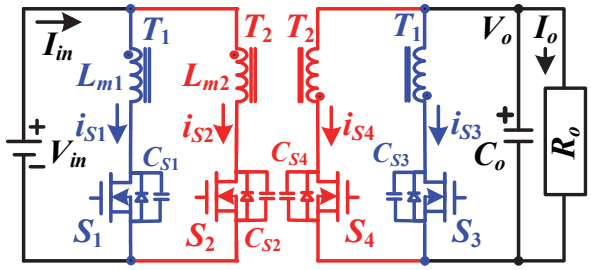


Fig. 2 Circuit schematic of the studied interleaved flyback converter.

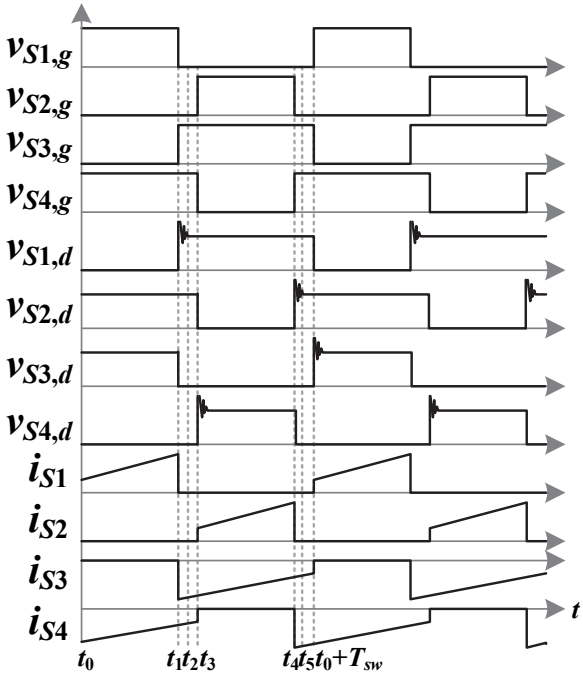


Fig. 3 Main waveforms under forward power flow.

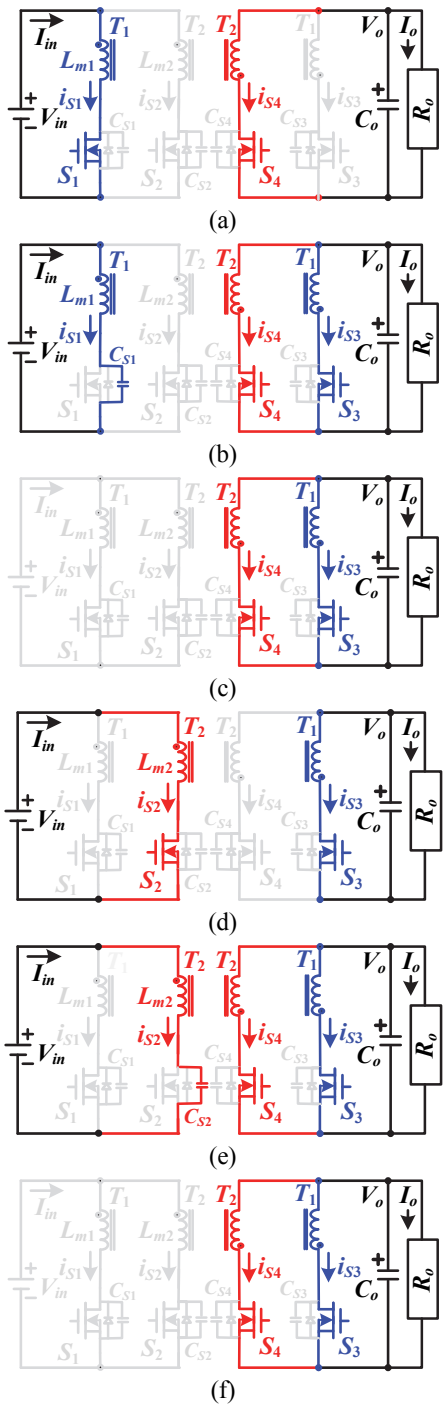


Fig. 4 Equivalent circuits of the operating stages in the developed circuit (a) stage 1 (b) stage 2 (c) stage 3 (d) stage 4 (e) stage 5 (f) stage 6.

Stage 1 [$t_0 \sim t_1$]: Before stage 1, both active devices S_1 and S_2 are inactive and the energy on L_{m1} and L_{m2} are released to Ro through the synchronous rectifiers S_3 and S_4. After time t0, S_1 is active and synchronous rectifier S_3 is inactive. The primary and secondary voltages of T_1 are $v_{Lm1} = V_{in}$ and v_{T1}, $s = V_{in}/n$. Therefore, the primary current $i_{Lm1}(t) = i_{S1}(t)\ i_{Lm1}(t_0) + V_{in}(t\text{-}t_0)/L_{m1}$. The input energy is stored on Lm1 in this stage. The voltage stress of the synchronous rectifier S_3 approximates $V_{in}/n + V_o$. The energy stored on L_{m2} is continuously discharged to the output load R_o and the secondary winding current is continuously decreased as $i_{S4}(t) \approx i_{S4}(t_0) + V_o(t\text{-}t_0)/(n^2 L_{m2})$. The voltage stress of the switch S_2 approximates $V_{in} + n_{Vo}$.

Stage 2 [$t_1 \sim t_2$]: At the beginning of this stage, S_1 is inactive and the synchronous rectifier S_3 becomes active at time t_1. The positive primary current i_{S1} flows through the leakage inductor $L_{lk,\,T1}$ and the output capacitor C_{S1} of switch S_1. The resonant frequency is $f_r = 1/2\pi\sqrt{L_{lk,T1}C_{S1}}$; thus, there is a voltage spike occurring on the drain-to-source voltage of S_1. This spike voltage is normally greater than the secondary side voltage reflected to the primary side n_{Vo}. In order to avoid damaging the power switch S_1, an RCD snubber is usually connected in parallel to the primary terminal T_1. The energy at $L_{lk,\,T1}$ is completely discharged at time t_2.

Stage 3 [$t_2 \sim t_3$]: The switch current i_{S1} decreases to zero at time t_2, whereupon the energy at L_{m1} is output to R_o, through S_3. At this stage, the secondary currents are increased and can be expressed by $i_{S3}(t) \approx i_{S3}(t_2) + V_o(t\text{-}t_2)/(n^2 L_{m1})$ and $i_{S4}(t) \approx i_{S4}(t_2) + V_o(t\text{-}t_2)/(n^2 L_{m2})$. At this time, the theoretical voltage rating of S_1 and S_2 is given by $V_{in} + n_{Vo}$.

Stage 4 [$t_3 \sim t_4$]: At time t_3, S_2 and S_4 are active and inactive, respectively. Inductor voltage is $v_{Lm2} = V_{in}$, the primary current can be described by $i_{Lm2}(t) = i_{S2}(t) \approx i_{Lm2}(t_3) + V_{in}(t\text{-}t_3)/L_{m2}$, the secondary winding voltage is given by $v_{T2,\,s} = V_{in}/n$, and the voltage stress of S_4 is $v_{S4,\,ds} = V_{in}/n + V_o$, the secondary side current is $i_{S3}(t) \approx i_{S3}(t_3) + V_o(t\text{-}t_3)/(n^2 L_{m1})$, and the voltage stress of S_1 is $v_{S1,\,ds} = V_{in} + n_{Vo}$. Input power is stored on L_{m2} and the energy stored on L_{m1} is discharged to the output load R_o.

Stage 5 [$t_4 \sim t_5$]: At the beginning of stage 5, S_2 turns off and S_4 turns on. i_{S2} flows through the leakage inductor $L_{lk,\,T2}$ and the output capacitor C_{S2} of S_2. $L_{lk,\,T2}$ and C_{S2} are resonant, so that a voltage spike occurs at C_{S2}. The RCD snubber can be adopted to limit voltage spikes and avoid damage to the switch S_2. At time t_5, the energy stored on $L_{lk,\,T2}$ is fully discharged; thus, $i_{S2} = 0$ and $v_{S2,\,ds} = V_{in} + n_{Vo}$.

Stage 6 [$t_5 \sim t_0 + T_{sw}$]: At t_5, the energy stored on $L_{lk,\,T2}$ is completely discharged and $i_{S2} = 0$. In this stage, the energy stored on L_{m1} and L_{m2} is discharged to output load R_o through S_3 and S_4 respectively. The secondary side currents $i_{S3}(t) \approx i_{S3}(t_5) + V_o(t\text{-}t_5)/(n^2 L_{m1})$ and $i_{S4}(t) \approx i_{S4}(t_5) + V_o(t\text{-}t_5)/(n^2 L_{m2})$ and the voltage ratings of S_1 and S_2 are limited at $V_{in} + n_{Vo}$.

When S_3 and S_4 are operated as the main power switches with interleaved pulse-width modulation, and S_1 and S_2 serve as synchronous rectifiers, then reverse power flow is achieved from the low voltage side to the input DC bus. The circuit operations in this power flow are the same as the discussions in the above paragraph. Therefore, there are not described and discussed again.

3. CIRCUIT CHARACTERISTICS

The interleaved duty-cycle control is adopted to control S_1 ~ S_4 and V_o. The interleaved flyback circuit tested is operated using CCM. When S_1 is active and S_3 is inactive, the current variation on the primary side of T_1 is calculated by (1).

$$\Delta i_{S_1} = V_{in} dT_{sw} / L_m \tag{1}$$

Likewise, current variation on the secondary side of T_1 is calculated by (2) when S_1 is inactive and S_3 is active.

$$\Delta i_{S_3} = V_o (1-d) T_{sw} / (L_m / n^2) \tag{2}$$

The flux variation at transformer L_{m1} is zero in a complete switching cycle, in a steady-state. Therefore, it can be derived by $\Delta i_{s1} = \Delta i_{s3} / n$ and the voltage gain of the adopted circuit can be calculated by (3).

$$G_{DC} = \frac{V_o}{V_{in}} = \frac{d}{n(1-d)} \tag{3}$$

When S_1 or S_2 is active, the ripple current on L_{m1} or L_{m2} can be calculated as.

$$\Delta i_{Lm1} = \Delta i_{Lm2} = \frac{V_{in} dT_{sw}}{L_m} \tag{4}$$

The peak values of switches S_1 ~ S_4 are obtained by (5) and (6).

$$i_{S1,peak} = i_{S2,peak} \approx \frac{I_o}{2n(1-d)} + \frac{V_{in} dT_{sw}}{2L_m} \tag{5}$$

$$i_{S3,peak} = i_{S4,peak} \approx \frac{I_o}{2(1-d)} + \frac{nV_{in} dT_{sw}}{2L_m} \tag{6}$$

The root mean square values of i_{S1} ~ i_{S4} are related to duty cycle d and load current and is calculated by Eqs. (7) and (8).

$$i_{S1,rms} = i_{S2,rms} \approx \frac{I_o \sqrt{d}}{2n\,(1-d)} \tag{7}$$

$$i_{S3,rms} = i_{S4,rms} \approx \frac{I_o}{2\sqrt{1-d}} \tag{8}$$

Therefore, conduction losses in the switches S_1 ~ S_4 are given by (9) and (10).

$$P_{S1,con} = P_{S2,con} \approx \frac{r_{ds,on} dI_o^2}{4n^2\,(1-d)^2} \tag{9}$$

$$P_{S3,con} = P_{S4,con} \approx \frac{r_{ds,on} I_o^2}{4\,(1-d)} \tag{10}$$

where $r_{ds,\,on}$ is turn-on resistance at S_1 ~ S_4. The switching losses of the powered devices S_1 ~ S_4 are a function of voltage stress, switching frequency and output capacitance of the power switch.

$$P_{S1,sw} = P_{S2,sw} \approx f_{sw} C_o v_{ds,S1}^2 = f_{sw} C_o (V_{in} + nV_o)^2 \tag{11}$$

$$P_{S3,sw} = P_{S4,sw} \approx f_{sw} C_o v_{ds,S3}^2 = f_{sw} C_o (V_o + V_{in} / n)^2 \tag{12}$$

At the boundary condition mode for the flyback converter, it can be obtained the DC current through the magnetizing inductance is equal to $\Delta i_{Lm}/2$. Based on the boundary load current I_{oB}, the magnetizing inductance L_m can be calculated by (13).

$$L_{m1} = L_{m2} = L_m = \frac{n^2 (1-d)^2 V_o}{I_{oB} f_{sw}} \tag{13}$$

The copper losses in the transformers T_1 and T_2 are expressed by:

$$P_{T1,copper} \approx \frac{r_{T1,p} dI_o^2}{4n^2 (1-d)^2} + \frac{r_{T1,s} I_o^2}{4(1-d)} \approx \frac{r_{T1,p} I_o^2}{4n^2 (1-d)^2} \tag{14}$$

$$P_{T2,copper} \approx \frac{r_{T2,p} dI_o^2}{4n^2 (1-d)^2} + \frac{r_{T2,s} I_o^2}{4(1-d)} \approx \frac{r_{T2,p} I_o^2}{4n^2 (1-d)^2} \tag{15}$$

where $r_{T1,\,p}$, $r_{T1,\,s}$, $r_{T2,\,p}$ and $r_{T2,s}$ are copper resistances of T_1 and T_2 on the primary and secondary sides. If the allowed ripple voltage $\Delta V_{Co,\,esr}$ on the equivalent series resistance (ESR) of C_o is given, then the ESR value $rC_{o,\,esr}$, can be calculated by:

$$r_{Co,esr} \approx \frac{\Delta V_{Co,esr} (1-d)}{I_o} \tag{16}$$

Normally, the power loss on $r_{Co,\,esr}$ is significantly smaller than the power losses for switches and inductors; thus, the ESR loss at C_o can be considered negligible and disregarded.

4. DESIGN PROCEDURE AND TEST RESULTS

A 400 W prototype circuit is laid out in this section to demonstrate the effective properties of the novel interleaved flyback circuit. The bipolar voltage system links a 190 V DC microgrid to a 48 V output and the switching frequency is 65 kHz. The assumed duty cycle of the main switches S_1 and S_2 are 0.45 and the estimated converter efficiency is 90%. The turn-ratio of T_1 and T_2 is obtained by:

$$n = \frac{\eta d V_{in}}{(1-d) V_o} = \frac{0.9 \times 0.45 \times 190}{(1-0.45) \times 48} \approx 2.91 \tag{17}$$

The boundary load current selected was 80% of load current, to reduce magnetizing inductance. The actual turn-ratio used in this circuit prototype was $n = 3$. Therefore, the necessary magnetizing inductances L_{m1} and L_{m2} can be calculated by (18):

$$L_{m1} = L_{m2} = \frac{n^2 (1-d)^2 V_o}{I_{oB} f_{sw}} = \frac{3^2 \times (1-0.45)^2 \times 48}{0.8 \times \frac{400}{48} \times 65 \times 10^3} \approx 0.3 mH \tag{18}$$

Following (18), EER 42 cores with n_p = 36 turns, n_s = 12 turns, $L_{m,\,p}$ = 0.3mH, $L_{m,\,s}$ = 0.033mH, r_p = 450mΩ and r_p = 50mΩ were adopted for transformers T_1 and T_2. The basic copper losses on T_1 and T_2 were obtained by:

$$P_{T1,copper} = P_{T2,copper} = \frac{r_{T1,p} I_o^2}{4n^2 (1-d)^2} = \frac{0.45 \times (400/48)^2}{4 \times 3^2 (1-0.45)^2} \approx 2.87\ W \tag{19}$$

Since the core loss table or equation were not available in this laboratory, the core losses and copper losses of the transformers were assumed to be the same. The ripple currents through L_{m1} and L_{m2} were calculated by (20):

$$\Delta i_{Lm1} = \Delta i_{Lm2} = \frac{V_{in} d}{L_m f_{sw}} = \frac{190 \times 0.45}{0.3 \times 10^{-3} \times 65 \times 10^3} \approx 4.38A \tag{20}$$

The current stresses and the root-mean-square values of the powered devices $S_1 \sim S_4$ were calculated as follows:

$$i_{S1,peak} = i_{S2,peak} \approx \frac{I_o}{2n(1-d)} + \frac{V_{in} d T_{sw}}{2L_m} \approx 4.72A \tag{21}$$

$$i_{S3,peak} = i_{S4,peak} \approx \frac{I_o}{2(1-d)} + \frac{nV_{in} d T_{sw}}{2L_m} \approx 14.15A \tag{22}$$

$$i_{S1,rms} = i_{S2,rms} = \frac{I_o \sqrt{d}}{2n(1-d)} = \frac{(400/48) \times \sqrt{0.45}}{2 \times 3 \times (1-0.45)} \approx 1.7A \tag{23}$$

$$i_{S3,rms} = i_{S4,rms} \approx \frac{I_o}{2\sqrt{1-d}} = \frac{400/48}{2\sqrt{1-0.45}} \approx 5.6A \tag{24}$$

If the voltage spike on a leakage inductor can be ignored, the theoretical voltage ratings of $S_1 \sim S_4$ are expressed by (25) and (26).

$$v_{S1,rating} = v_{S2,rating} \approx V_{in} + nV_o = 190 + 3 \times 48 = 334V \tag{25}$$

$$v_{S3,rating} = v_{S4,rating} \approx V_o + V_{in}/n = 48 + 190/3 \approx 112V \tag{26}$$

ST Microelectronics STP35N60DM2 power MOSFET with V_{DSS} = 600 V, I_D = 28 A, $r_{ds,\,on}$ = 0.22Ω and C_o = 300 pF were selected for power switches $S1$ and $S2$. MOSFET SM1F01NF with V_{DSS} = 150 V, I_D = 80 A, $r_{ds,\,on}$ = 32 mΩ and C_o = 600 pF were selected for power switches S_3 and S_4. Based on the selected power MOSFETs, the approximate power losses of $S_1 \sim S_4$ were calculated by (27) and (28).

$$\begin{aligned} P_{S1,loss} &= P_{S2,loss} = P_{S1,con} + P_{S1,sw} \\ &\approx \frac{r_{ds,on} d I_o^2}{4n^2(1-d)^2} + f_{sw} C_o (V_{in} + nV_o)^2 \approx 2.81W \end{aligned} \tag{27}$$

$$\begin{aligned} P_{S3,loss} &= P_{S4,loss} = P_{S3,con} + P_{S3,sw} \\ &\approx \frac{r_{ds,on} I_o^2}{4(1-d)} + f_{sw} C_o (V_o + V_{in}/n)^2 \approx 1.5W \end{aligned} \tag{28}$$

The output ripple voltage was assumed to be 1% of the nominal output voltage. The maximum equivalent series resistance of C_o was calculated by:

$$\begin{aligned} r_{Co,esr} &\le \frac{\Delta V_{Co,esr}(1-d)}{I_o} \\ &= \frac{0.01 \times 48 \times (1-0.45)}{400/48} \approx 0.0317\Omega \end{aligned} \tag{29}$$

Selecting C_o = 1360 μF/100 V gives $r_{Co,\,esr}$ = 10 mΩ. Disregarding power losses on $r_{Co,\,esr}$, leakage inductance of transformers and the snubber circuit, the theoretical circuit efficiency at full load can be estimated by:

$$\begin{aligned} \eta &= \frac{P_o}{P_o + 2P_{S1,loss} + 2P_{S3,loss} + 4P_{T1,copper}} \\ &= \frac{400}{400 + 2 \times 2.81 + 2 \times 1.5 + 4 \times 2.87} = 95.2\% \end{aligned} \tag{30}$$

The small-signal transfer function from control voltage to output voltage, operating under voltage control mode with CCM, can be defined by:

$$G_p(f) = \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{V_{in}}{nV_p(1-d)^2} \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 - \frac{s}{\omega_{z,RHP}}\right)}{1 + \frac{s^2}{\omega_o^2} + \frac{s}{\omega_o} \cdot \frac{1}{Q}} \tag{31}$$

where, $V_p = 1, f_o = (1-d)\, n / 2\pi \sqrt{L_{m,p} C_o} \approx 411$ kHz , $f_z = 1 / 2\pi C_o r_c \approx 11.7$ kHz, $f_{z,\,RHP} = (1-d)^2 R_o n^2 / (2\pi L_{m,\,p} d) \approx 18.5$ kHz, and $Q = (1-d)^2 R_o n^2 / (\omega_o L_{m,\,p}) \approx 20.2$. Using the derived circuit parameters from the previous section, the transfer function in (31) can be rewritten as:

$$G_p(f) = \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = 209.37 \times \frac{\left(1 + j\frac{f}{11700}\right)\left(1 - j\frac{f}{18500}\right)}{1 - \frac{f^2}{411^2} + j\frac{f}{411} \cdot \frac{1}{20.2}} \tag{32}$$

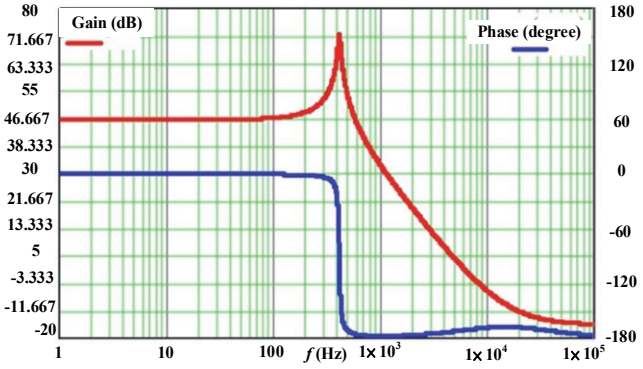


Fig. 5 Bode plot of the small-signal transfer function $G_p(f)$ from control signal to output voltage, for the interleaved flyback converter.

Figure 5 shows the Bode plot of the small-signal transfer function, from control signal to output voltage. A type III voltage controller was used to control the load voltage. The cutoff frequency fc was set to 5 kHz as that is below f_{sw}/10. Since the pole frequency and zero frequency of the transfer functions were f_o = 411 Hz and f_z = 11.7 kHz, the double zero frequency of the controller was $f_{z1,\,c} = f_{z2,\,c} = f_o$ = 411 Hz, one pole frequency was tuned to $f_{p1,\,c} = f_z$ = 11.7 kHz and the other was tuned to $f_{p2,\,c} = f_{sw}$ = 65 kHz. The control transfer function of the standard type III controller can thus be calculated by (33):

$$G_c(s)=\frac{\hat{v}_c(s)}{\hat{v}_o(s)}=-\frac{1}{\frac{s}{\omega_{Pi,c}}}\frac{\left(1+\frac{s}{\omega_{z1,c}}\right)\left(1+\frac{s}{\omega_{z2,c}}\right)}{\left(1+\frac{s}{\omega_{p1,c}}\right)\left(1+\frac{s}{\omega_{p2,c}}\right)} \quad (33)$$

$$=-\frac{1}{\frac{jf}{f_{Pi,c}}}\frac{\left(1+j\frac{f}{411}\right)\left(1+j\frac{f}{411}\right)}{\left(1+j\frac{f}{11700}\right)\left(1+j\frac{f}{65000}\right)}$$

At the cutoff frequency f_c, the control-to-output gain $|G_p(f_c)|$ is expressed by:

$$|G_p(f_c)|=209.37\times\frac{\sqrt{1+\left(\frac{5000}{11700}\right)^2}\sqrt{1+\left(\frac{5000}{18500}\right)^2}}{\sqrt{\left(1-\frac{5000^2}{411^2}\right)^2+\left(\frac{5000}{411}\cdot\frac{1}{20.2}\right)^2}} \quad (34)$$

$$=1.60446=4.1066dB$$

Due to loop gain $|G_L(f_c)| = |G_p(f_c)| \times |G_c(f_c)| = 1$ or 0 dB at the cutoff frequency f_c, the $f_{pi,c}$ value can be calculated by:

$$|G_L(f_c)|=209.37\times\frac{\sqrt{1+\left(\frac{5000}{11700}\right)^2}\sqrt{1+\left(\frac{5000}{18500}\right)^2}}{\sqrt{\left(1-\frac{5000^2}{411^2}\right)^2+\left(\frac{5000}{411}\cdot\frac{1}{20.2}\right)^2}} \quad (35)$$

$$\times\frac{1}{\frac{5000}{f_{Pi,c}}}\frac{\sqrt{1+\left(\frac{5000}{411}\right)^2}\sqrt{1+\left(\frac{5000}{411}\right)^2}}{\sqrt{1+\left(\frac{5000}{11700}\right)^2}\sqrt{1+\left(\frac{5000}{65000}\right)^2}}=1$$

$$f_{Pi,c}=\frac{5000\sqrt{1+\left(\frac{5000}{11700}\right)^2}\sqrt{1+\left(\frac{5000}{65000}\right)^2}}{209.37\sqrt{1+\left(\frac{5000}{411}\right)^2}\sqrt{1+\left(\frac{5000}{411}\right)^2}} \quad (36)$$

$$\times\frac{\sqrt{\left(1-\frac{5000^2}{411^2}\right)^2+\left(\frac{5000}{411}\cdot\frac{1}{20.2}\right)^2}}{\sqrt{1+\left(\frac{5000}{11700}\right)^2}\sqrt{1+\left(\frac{5000}{18500}\right)^2}}\approx 22.8Hz$$

The controller gains at the zero frequency $f_{z2,c}$ and pole frequency $f_{p1,c}$ are calculated by (37) and (38), respectively.

$$A_L(f_{z1,c})=G_C(f_c)+20log\left(\frac{f_{z1,c}}{f_c}\right) \quad (37)$$

$$=-4.1066dB+(-21.7026dB)=0.05123$$

$$A_H(f_{p1,c})=G_C(f_c)+20log\left(\frac{f_{p1,c}}{f_c}\right) \quad (38)$$

$$=-4.1066dB+(7.3843dB)=1.45843$$

A TL431 adjustable shunt regulator and a photocoupler PC817 were used to provide type III control. The PWM integrated circuit UCC28221 was introduced to provide the necessary interleaved PWM operation. Based on $G_p(f)$ and $G_c(f)$, the loop gain $G_L(f)$ of this converter can be determined by:

$$G_L(f)=-\frac{4773.636}{jf}\times\frac{\left(1+j\frac{f}{11700}\right)\left(1-j\frac{f}{18500}\right)}{1-\frac{f^2}{411^2}+j\frac{f}{411}\cdot\frac{1}{20.2}} \quad (39)$$

$$\times\frac{\left(1+j\frac{f}{411}\right)\left(1+j\frac{f}{411}\right)}{\left(1+j\frac{f}{11700}\right)\left(1+j\frac{f}{65000}\right)}$$

The phase of the negative loop gain $-G_L(f)$ is obtained from:

$$\angle -G_L(f)=tan^{-1}\left(\frac{f}{11700}\right)-tan^{-1}\left(\frac{f}{18500}\right)$$

$$-tan^{-1}\left(\frac{\frac{f}{411}\times\frac{1}{20.2}}{1-\frac{f^2}{411^2}}\right)-90^0+tan^{-1}\left(\frac{f}{411}\right) \quad (40)$$

$$+tan^{-1}\left(\frac{f}{411}\right)-tan^{-1}\left(\frac{f}{11700}\right)-tan^{-1}\left(\frac{f}{65000}\right)$$

The magnitude and phase of the loop gain, $|G_L(f)|$ and $\angle$-$G_L(f)$, are shown in Fig. 6. Based on the simulated results from Fig. 6, the adopted converter has a 61 degree phase margin, and a -12 dB gain margin.

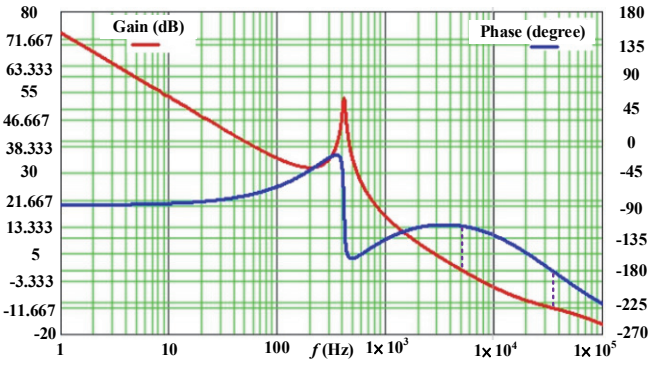


Fig. 6 Bode plot of $|G_L(f)|$ and $\angle$-$G_L(f)$ of the loop gain for the interleaved flyback converter.

This section presents findings of the tested circuit that provides a 400 W output load under a 190 V input with a 48 V output. Figs. 7-9 show the test waveforms of the converter under a power flow from 190 V to 48 V. Similarly, the adopted circuit

can also function using a reverse power flow, from 48 V to 190 V, as shown in Figs. 10-12. Figure 7 illustrates the test waveforms of the power switches S_1 and S_2 and the synchronous rectifiers S3 and S4 under a 50% load at the rated power level. From the test results, it can be seen that the gating signal at S_2 (S_4) is phase-shifted with respective to S_1 (S_3), by $T_{sw}/2$. Similarly, the gating waveforms of S_3 (S_4) and S_1 (S_2) are complementary with a dead time. Figure 8 demonstrates the test waveforms of main switches S_1 and S_2 under 50% power and at the rated power level. The primary side currents i_{S1} and i_{S2} are interleaved. It can be seen that the tested interleaved flyback circuit is controlled by CCM at the rated power level; however, the circuit operates in discontinuous conduction mode at 50% power. When the circuit is running in discontinuous conduction mode, $iS1$ and i_{S2} increase from their negative values, due to the synchronous rectifier continuously conducting at the OFF time interval determined by S_1 and S_2. Test waveforms of the synchronous rectifiers S_3 and S_4 under 50% power and at the rated power level are provided in Fig. 9. i_{S3} and i_{S4} are negative due to the direction of the current load. Figs. 10-12 show the test waveforms of the adopted converter operating with a reverse power flow, from 48 V to 190 V. The measured waveforms in Figs. 10-12, under reverse power flow, are similar to the measured waveforms in Figs. 7-9 under forward power flows. The measured circuit efficiencies were 85.2% (20% load), 90.9% (50% load) and 91.3% (100% load) under forward power flow, and 88% (20% load), 93.7% (50% load) and 92.3% (100% load) under reverse power flow.

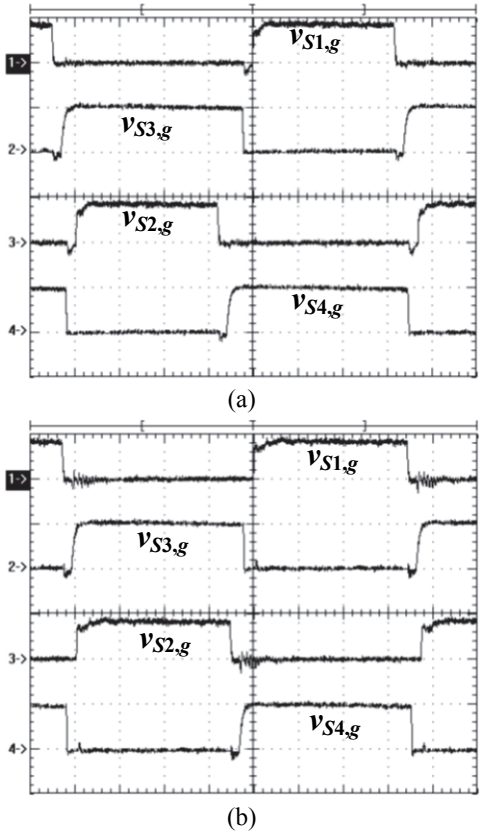


Fig. 7 **Test results of $v_{S1,g} \sim v_{S4,g}$ (a) at 50% power (b) at rated power [$v_{S1,g} \sim v_{S4,g}$: 10V/div; time: 2μs/div].**

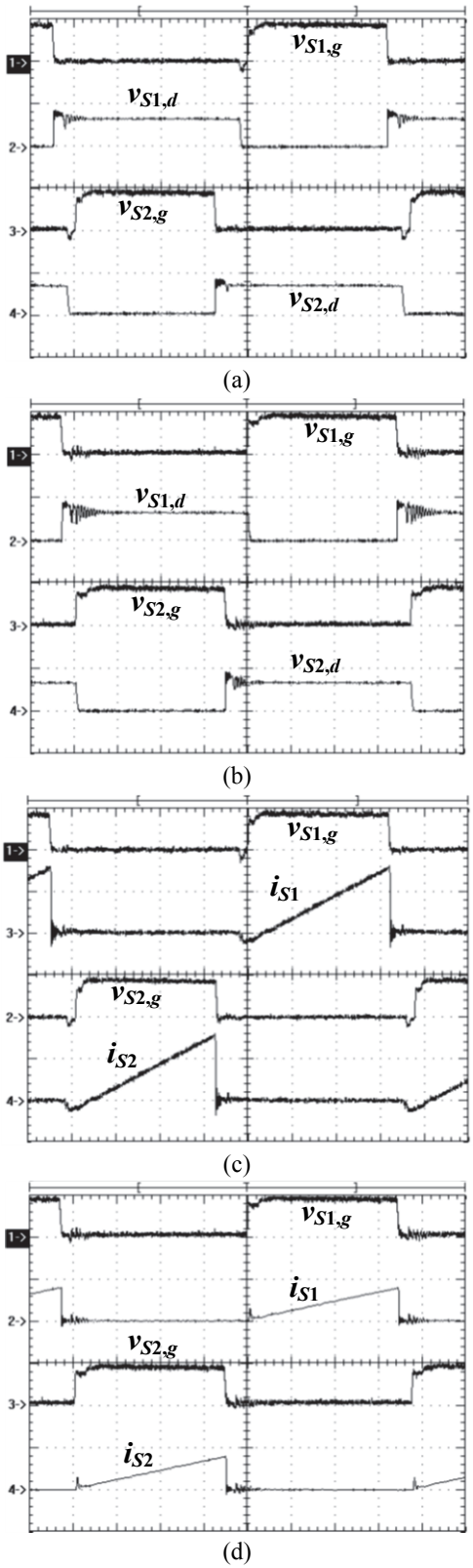


Fig. 8 **Test results of the main switches S_1 and S_2 (a) $v_{S1,g}$, $v_{S2,g}$, $v_{S1,d}$, $v_{S2,d}$ at 50% load (b) $v_{S1,g}$, $v_{S2,g}$, $v_{S1,d}$, $v_{S2,d}$ at rated load [$v_{S1,g}$, $v_{S2,g}$: 10V/div; $v_{S1,d}$, $v_{S2,d}$: 500V/div; time: 2μs/div] (c) $v_{S1,g}$, $v_{S2,g}$, i_{S1}, i_{S2} at 50% load [$vS1,g$, $v_{S2,g}$: 10V/div; i_{S1}, i_{S2}: 2A/div; time: 2μs/div] (d) $v_{S1,g}$, $v_{S2,g}$, i_{S1}, i_{S2} at rated load [$v_{S1,g}$, $v_{S2,g}$: 10V/div; i_{S1}, i_{S2}: 5A/div; time: 2μs/div].**

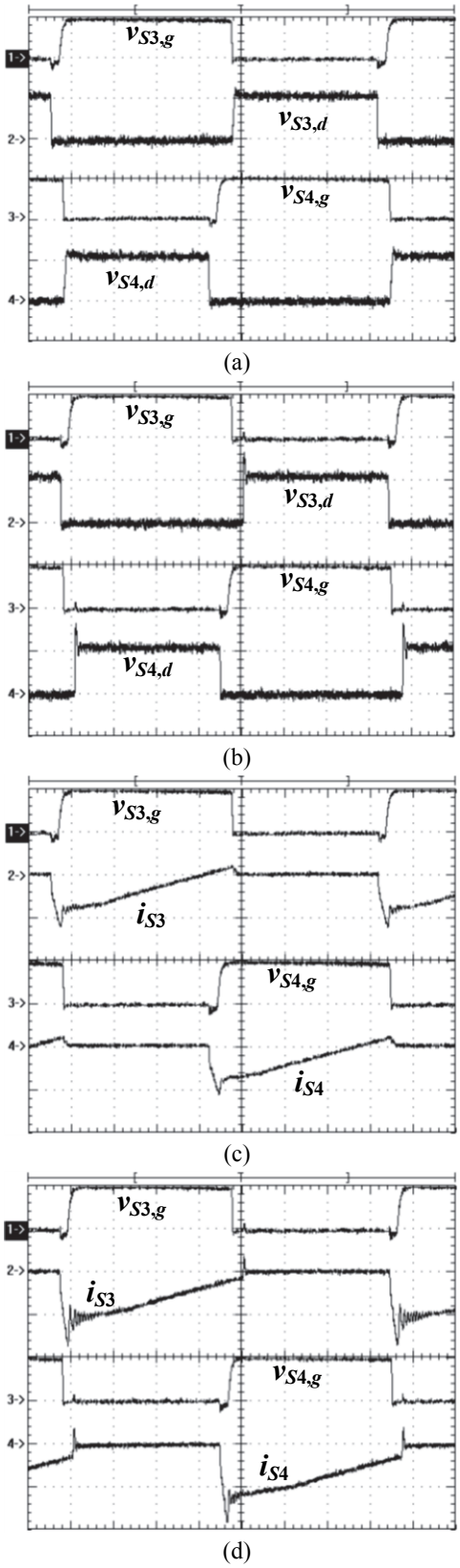


Fig. 9 Test results of the synchronous rectifiers S_3 and S_4 (a) $v_{S3,g}$, $v_{S4,g}$, $v_{S3,d}$, $v_{S4,d}$ at 50% load (b) $v_{S3,g}$, $v_{S4,g}$, $v_{S3,d}$, $v_{S4,d}$ at rated load [$v_{S1,g}$, $v_{S2,g}$: 10V/div; $v_{S1,d}$, $v_{S2,d}$: 100V/div; time: 2μs/div] (c) $v_{S3,g}$, $v_{S4,g}$, i_{S3}, i_{S4} at 50% load (d) $v_{S3,g}$, $v_{S4,g}$, i_{S3}, i_{S4} at rated load [$v_{S3,g}$, v_{S4}, g: 10V/div; i_{S3}, i_{S4}: 10A/div; time: 2μs/div].

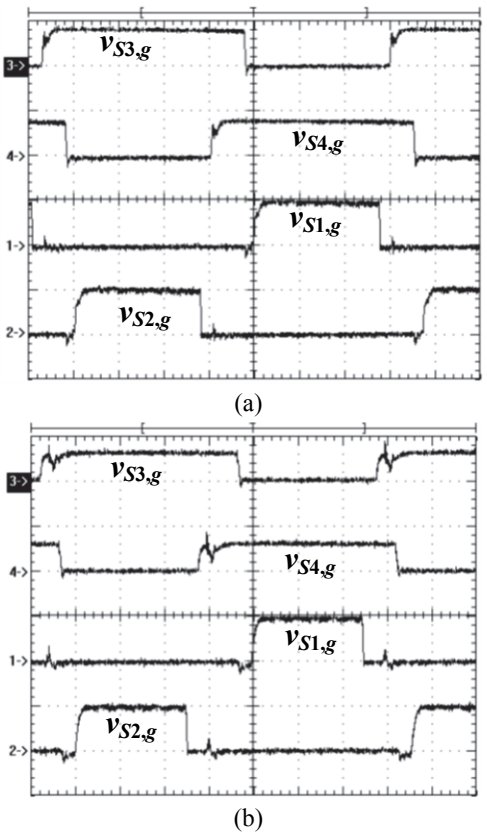
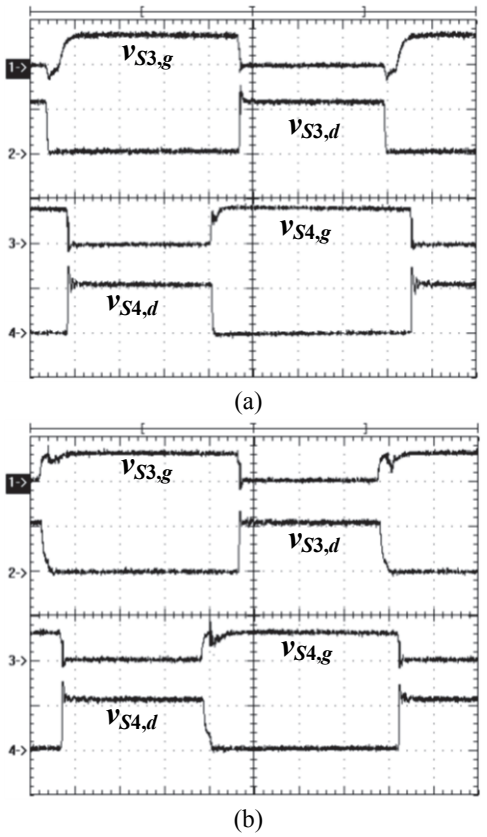
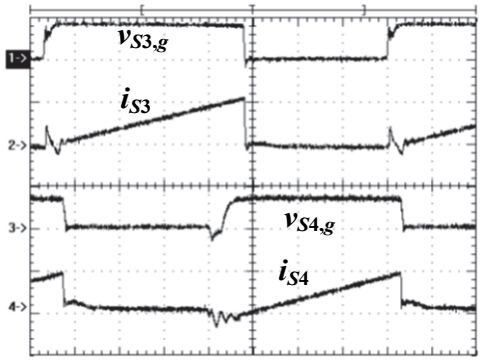
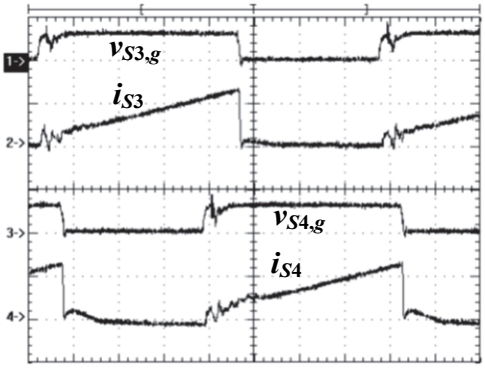


Fig. 10 Test results of $S_1 \sim S_4$ under reverse power, from 48 V to 190 V (a) at 50% load (b) at rated load [$v_{S1,g} \sim v_{S4,g}$: 10V/div; time: 2μs/div].



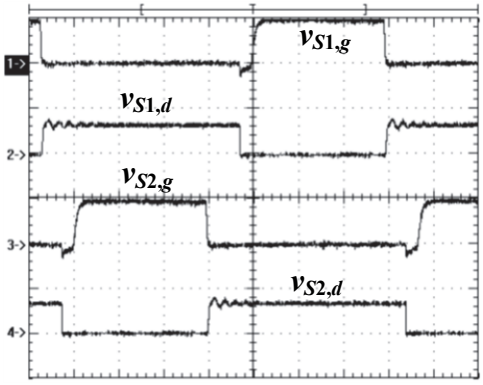


(c)

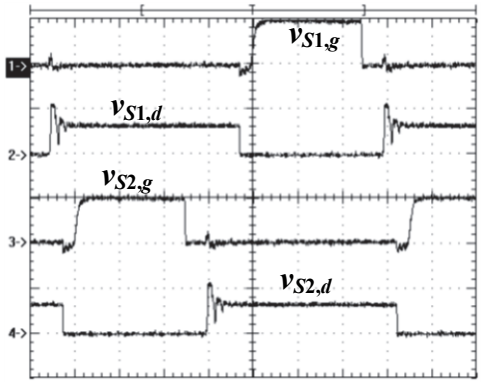


(d)

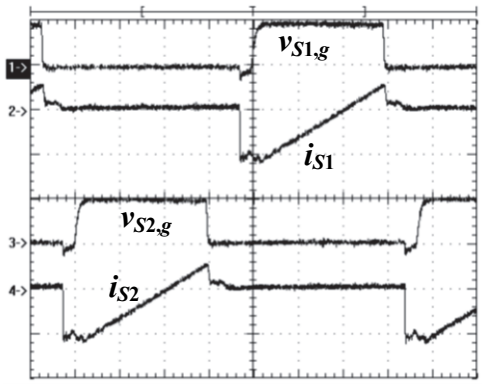
Fig. 11 Test results of the main switches *S*3 and *S*4 under reverse power (a) $v_{S3,g}$, $v_{S4,g}$, $v_{S3,d}$, $v_{S4,d}$ at 50% load (b) $v_{S3,g}$, $v_{S4,g}$, $v_{S3,d}$, $v_{S4,d}$ at rated load [$v_{S3,g}$, $v_{S4,g}$: 10V/div; $v_{S3,d}$, $v_{S4,d}$: 100V/div; time: 2μs/div] (c) $v_{S3,g}$, $v_{S4,g}$, i_{S3}, i_{S4} at 50% load (d) $v_{S3,g}$, $v_{S4,g}$, i_{S3}, i_{S4} at rated load [$v_{S3,g}$, v_{S4}, *g*: 10V/div; i_{S3}, i_{S4}: 10A/div; time: 2μs/div].



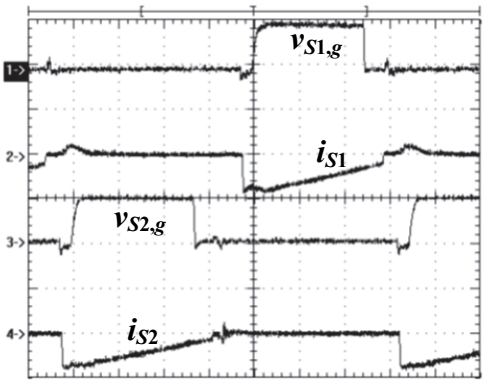
(a)



(b)



(c)



(d)

Fig. 12 Test results of the synchronous rectifiers S_1 and S_2 under reverse power from (a) $v_{S1,g}$, $v_{S2,g}$, $v_{S1,d}$, v_{S2},d at 50% load (b) $v_{S1,g}$, $v_{S2,g}$, $v_{S1,d}$, $v_{S2,d}$ at rated load [$v_{S1,g}$, $v_{S2,g}$: 10V/div; $v_{S1,d}$, $v_{S2,d}$: 500V/div; time: 2μs/div] (c) $v_{S1,g}$, $v_{S2,g}$, i_{S1}, i_{S2} at 50% load [$v_{S1,g}$, $v_{S2,g}$: 10V/div; i_{S1}, i_{S2}: 2A/div; time: 2μs/div] (d) $v_{S1,g}$, $v_{S2,g}$, i_{S1}, i_{S2} at rated load [$v_{S1,g}$, $v_{S2,g}$: 10V/div; i_{S1}, i_{S2}: 5A/div; time: 2μs/div].

5. CONCLUSION

This paper presented a bidirectional interleaved flyback converter. The adopted circuit can be applied in a DC microgrid system, for small scale energy storage units in residential homes. The circuit topology of the adopted converter is simple and has a high circuit efficiency due to the use of MOSFETs, rather than fast recovery diodes. The interleaved PWM operation can decrease ripple currents at the input and output sides, increasing input and output ripple frequency. Therefore, less output capacitance can be selected on the load side. The circuit operation, principle operation and converter characteristics were discussed. The design procedures of the studied circuit were discussed and the circuit parameters were derived. Finally, the practicability of the converter was demonstrated, to validate the theoretical analysis. The measured results of the experimental waveforms showed that the theoretical analysis matched the practical implementation. Future research following this device will be to add an auxiliary circuit to reduce the voltage spike, and realize soft switching on power devices.

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