Journal of Innovative Technology, Vol. 2, No. 2, pp. 47-52, September 2020
http://doi.org/10.29424/JIT.202009_2(2).0008

Design and Implementation of a Low-cost Back-to-back Dynamic Voltage Restorer

Chao-Tsung Ma [1*] and Yi-Hung Tian [2]

ABSTRACT

The dynamic voltage restorer (DVR) is a power converter-based device widely used in power distribution systems to improve voltage quality. A conventional DVR includes an energy storage device (ESD) to provide the required power for a limited duration of voltage sag. However, the employment of ESD increases the DVR costs and limits its functionality. This research paper investigated a single-phase back-to-back DVR with simulation and small-scale hardware implementation. The proposed DVR includes two inverters connected in series and parallel with the distribution system, respectively, to enable bidirectional power flow. The advantage of this topology is its ability to compensate for longer voltage sags and swells, thus achieving a low-cost design. Using digital control scheme, the proposed DVR is able to perform multiple control functions simultaneously, including voltage swell/sag compensation, power factor correction (PFC), and harmonic current compensation. Based on the aforesaid, this paper reviews the related literature on DVR and then introduces the working principles of DVR and the proposed control scheme. Also, two sets of simulation studies and hardware tests were performed to do so. The typical results derived from the software simulation and small-scale hardware implementation are provided to verify the effectiveness of the proposed DVR and the related control scheme.

Keywords: Dynamic Voltage Restorer (DVR); power quality control; back-to-back converter; digital controller.

1. INTRODUCTION

In recent years, in response to the trends of energy conservation and carbon reduction emissions, the number of renewable power generation units has significantly increased. The implementation of the concept of Industry 4.0 and the rapid expansion of smart, automatic production equipment have caused power quality problems to become increasingly serious (Johnson and Hassan 2016; Ndirangu *et al*. 2018). Among those major issues most associated with the field of power quality, voltage sags and swells are two of the most serious concerns on the issue of sensitive loads. In this regard, the dynamic voltage restorer (DVR) has been widely recognized as an economical and efficient solution to this problem of voltage sag/swell. It has also been widely applied in this field to protect the sensitive loads from the blackout problems. Conventional DVRs (Farhadi-Kangarlu *et al*. 2017; İnci *et al*. 2017) are connected in series with the line through injection transformers and inject a desired voltage to help load voltage synchronize with grid supply voltage for real-time voltage sag/swell compensation. In addition, to increase the system efficiency, there is also a design scheme where the circuit topology does not use injection transformers (Ansal *et al*. 2016). Figure 1 describes the one-line diagram of a power distribution system with a DVR connected in series with the distribution system feeder via a transformer. When load 1 experiences a short-circuit fault, the voltage at the distribu tion feeder may drop rapidly, thereby causing the voltage supplied to load 2 to drop as well. The DVR installed in the feeder can immediately compensate for the voltage drop of load 2.

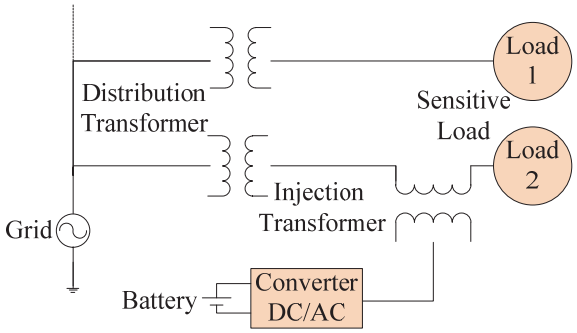

Fig. 1 One-line diagram of a power distribution system with a battery-based DVR.

In practice, during voltage sag or swell, the voltage of the DVR injection is used to restore the load voltage to a nominal value for accomplishing the control purposes. During the control operation, the DVR exchanges both active and reactive power with the feeder. In the case of voltage sag, the active power must be provided by the DVR. This is the main reason why the conventional DVRs use energy storage devices, such as batteries, supercapacitors, and flywheel energy storages connected to its DC bus. However, the energy storage devices increase system costs (Udayakiran and Vali 2017), and owing to the existence of the energy storage device, regular maintenance is required. Normally, the DVR requires a suitable controller to determine the phase and magnitude of the injected voltage to ensure the immediate recovery of the phase and amplitude of load voltage. The choices for compensation strategies of DVR are not unique. Dif-

Manuscript received July 30, 2020; accepted July 31, 2020.
[1*] Associate Professor (corresponding author), Department of EE, CEECS, National United University, Taiwan 36003, R.O.C. (e-mail: ctma@nuu.edu.tw).
[2] Postgraduate Student, Department of EE, CEECS, National United University, Taiwan 36003, R.O.C.

ferent types of compensation strategies require different phase-locked loop (PLL) implementation techniques (Yada and Murthy 2016; Yada and Murthy 2016). Therefore, the design of PLL and the application of control signals mainly depend on the compensation strategy used. As documented in literature, three most popular technologies are pre-sag voltage recovery compensation (Ali *et al*. 2014), zero active power compensation (Messiha *et al*. 2016), and in-phase voltage compensation (Li *et al*. 2016). As to pre-sag voltage recovery compensation, it is necessary to inject active and reactive power. The DVR detects the difference between post-sag and pre-sag voltages and injects the appropriate voltage to restore the magnitude and phase of the load voltage to their pre-sag values. The pre-sag phase compensation is able to lock the grid voltage phase before voltage sag happens. This compensation strategy is mainly used for loads considered sensitive to the voltage amplitude and phase angle, and it requires a relatively large injection voltage in the case of large phase shifts. The active power generated by DVR in zero active power compensation heavily depends on the angle between the load current and the injection voltage. These two vectors must always be controlled orthogonally to ensure that the DVR achieves zero active power injection, and only the reactive power is provided or absorbed by the DVR. However, in the case of a unity power factor (PF) load, the voltage sag compensation capability of this method is quite limited. For a load with lower PF, the voltage sag can be easily compensated without the need for active power injection. On the other hand, the compensation strategy applied in-phase voltage compensation is relatively simple. The PLL outputs the phase angle of the compensated grid voltage, which can be compensated with a minimum voltage injection. Thus, it should be noted that this technique requires active power exchange, and the power level is related to the magnitude of line current before the sag. By referring to the work of Ali *et al*. (2017), a power electronic transformer (PET)-based DVR was established aiming at mitigating both symmetrical and asymmetrical voltage sag/swell. Multilevel inverter architecture was used, and the PET provided advanced compensation functions and extra flexibility.

Following this introduction section, the design of the proposed single-phase DVR based on two back-to-back H-bridge inverters is addressed, followed by the DVR circuit topology and control scheme, case simulation and implementation results, and, finally, a conclusion.

2. DVR SYSTEM CONFIGURATION AND OPERATING PRINCIPLE

2.1 The proposed DVR operation principle

The proposed single-phase back-to-back DVR was composed of two inverters connected in parallel and series with the distribution feeder, respectively. The complete system block diagram is clearly shown in Fig. 2. The two inverters are connected by a common DC bus with a capacitor bank. The bypass switch is used to bypass the secondary side of the injection transformer when the voltage value of the grid is within allowable range. Under such a condition, the DVR is working in its standby mode to further reduce the system losses. Once the voltage is abnormal, the bypass switch will be opened, and the series inverter is activated to inject the voltage in series with the grid voltage. In the meantime, the parallel inverter provides the power exchange path required for the power balancing during the DVR compensation, and the voltage injection is performed through an injection transformer connected between the power source and the load.

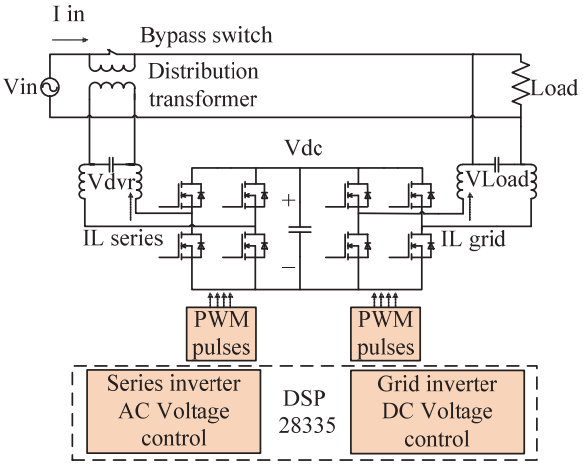

Fig. 2 The proposed DVR system block diagram.

In operation, during a voltage-sag even, parallel inverter was used to control DC bus voltage and operates as a unity PF rectifier. In order to ensure that the parallel inverter can be operated normally when facing a grid voltage fluctuation, the parallel inverter can be placed at the load end (after the series transformer). With this arrangement, the series inverter produces required AC compensation voltage, which is in phase with grid voltage, during the voltage sag. The active power required by the DVR is taken from the load side, and the energy flows from the parallel inverter to the series inverter. During the voltage swell, the power flows from the series inverter to the parallel inverter, which transmits the current to the load. In order to filter out the high frequency switching harmonics of the inverter, a suitable LC filter must be used at the output of each of the parallel and series inverters. This ensures that the current supplied to the grid from the series or parallel inverter has a relatively small amount of high frequency components. To provide a clear picture of the operating principle stated above, Figure 3 depicts the vector diagrams of the voltages during grid voltage sag and swell. As can be seen from Fig. 3, when a voltage sag occurs, the DVR injection voltage is in phase with the sag voltage, while, in contrast, when a voltage swell occurs, the injection voltage is reversed from the swell voltage to keep the load voltage constant.

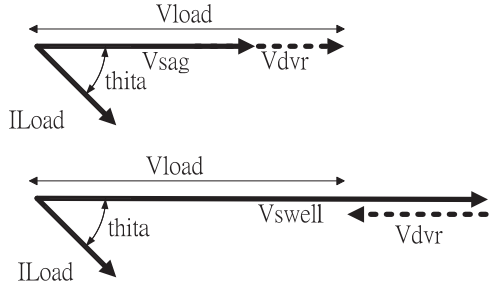

Fig. 3 Voltage compensation vector diagrams during voltage sag and swell.

2.2 The proposed DVR control scheme

The two inverters in the proposed back-to-back DVR used a dual-loop voltage and current control scheme. For the parallel inverter, the reference DC bus voltage is compared with the feedback voltage to produce an error signal, which can be processed via a PI controller to generate a reference current signal. This is then multiplied by a sinusoidal signal to produce a reference signal. This reference current signal is actually a sinusoidal signal with the same phase and frequency as the load voltage. The inner current controller was employed to ensure that the output AC current could follow its reference value. The overall control block diagram of the parallel inverter is shown in Fig. 4 (a). For the series inverter, its reference AC output voltage is determined by grid voltage and its nominal value. The reference AC voltage waveform can be processed by a set of properly designed voltage and current controllers to ensure that the injected voltage can quickly follow the voltage reference signal. The overall control block diagram of the series inverter is illustrated in Fig. 4 (b).

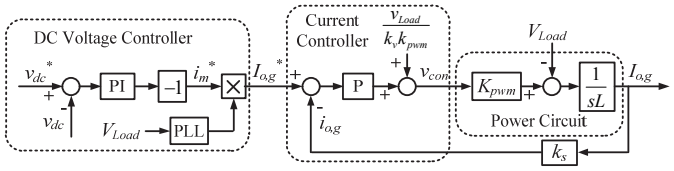

Fig. 4 (a) The overall control block diagram of the DVR parallel inverter.

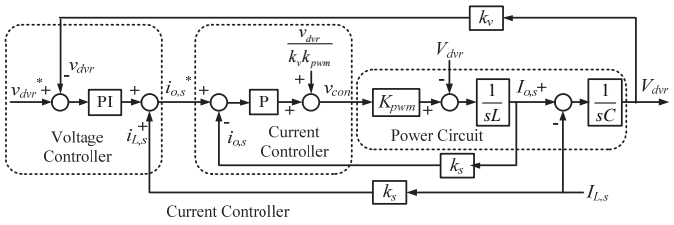

Fig. 4 (b) The overall control block diagram of the DVR series inverter.

2.3 Phase lock loop

Figure 5 shows the signal flow of the phase-locked loop (PLL) discussed in the previous section. A PLL was used to detect the phase angle and the frequency of the grid voltage. In abnormal situations, such as the voltage sag/swell, phase jump, and harmonics, these parameters are required to ensure that system performance meets the standards.

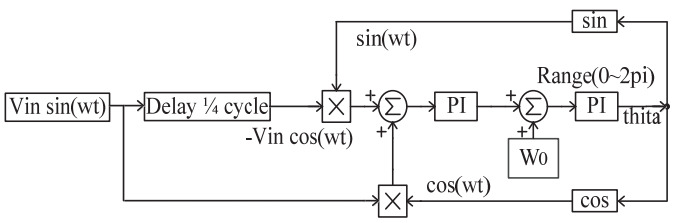

Fig. 5 The signal flow diagram of the proposed phase lock loop.

2.4 DVR system parameters

To demonstrate the feasibility and effectiveness of the proposed DVR, a test system was constructed. The turns ratio of the injection transformer of the single-phase DVR was 2:1; the single-phase inverter was rated at 1 kVA, 110 V_{rms}. The DVR compensation range was designed in the range of 55 V_{rms} to 165 V_{rms}. The power rating of the injection transformer depended on the voltage to be injected and the load current flowing through the secondary of the injection transformer. The current flowing through the secondary side of the injection transformer was the same as the load. In this design case, the injection voltage of the secondary side of the transformer was limited to 55 V_{rms}, so the rated power of the injection transformer could be much smaller than the load.

3. CASE SIMULATION AND EXPERIMENTAL RESULTS

3.1 System description and case simulations

In order to verify the proposed single-phase back-to-back DVR and the control strategy discussed above, this subsection presents the system description, PSIM modeling and detailed case simulation analyses of the proposed DVR. The main parameters of the DVR system and controllers are summarized in Tables 1 and 2 below.

Table 1 LC filter parameters of the DVR inverters.

Inverter	Inductor	Capacitor
Series inverter	1 mH	10 μF
Parallel inverter	1 mH	10 μF

Table 2 DVR controller parameters.

Inverter	Voltage loop (Kp & Ki)	Current loop (Kp)
Series inverter	PI (0.1267 & 0.00152)	P (2.7)
Parallel inverter	PI (2.2723 & 0.00272)	P (1.8)

Figure 6 shows the measuring positions and polarity definitions. V_{dc} represents the DC bus voltage, V_{dvr} is the series inverter injection voltage, V_{in} is the grid voltage, V_{Load} is load voltage, and I_{in} is the grid current flowing to the load, and I_{load} denotes load current.

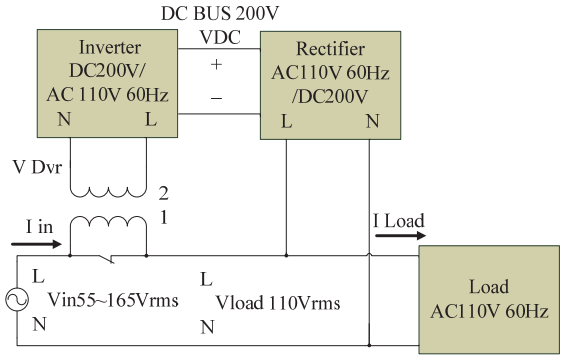

Fig. 6 DVR system connection configuration and the measuring points.

3.1.1 Case 1: Voltage sag/swell compensation

Regarding this case, the standard grid voltage value was set to 110 V (rms), and the load power was arranged at 363 W. Also, the assumed residual voltage during voltage sag was 80 V (rms), and the maximum voltage during voltage swell was 140 V (rms). With the proposed control scheme, one can observe whether the DVR series inverter can maintain the load voltage at the nominal voltage, 110 V (rms) while the grid-connected inverter maintains the DC BUS voltage at 200 V. Figure 7 shows the compensation results of the series inverter with the in-phase voltage injection during voltage sag. As we can see in Fig. 7, the real power flowed from the parallel inverter to the series inverter, causing I_{in} to increase.

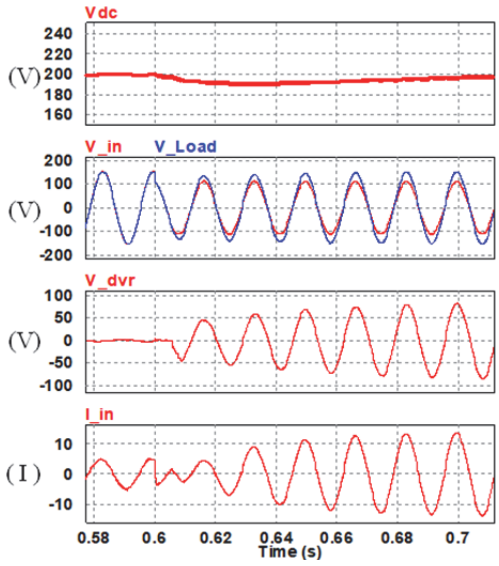

Fig. 7 Voltage sag simulation results (V_{in_rms} = 80 V, load = 363W).

Figure 8 shows the DVR control results of voltage swell. As can be seen from Fig. 8, the series inverter compensated a reverse voltage, and the active power flowed from the series inverter to the parallel inverter, causing I_{in} to slightly decrease.

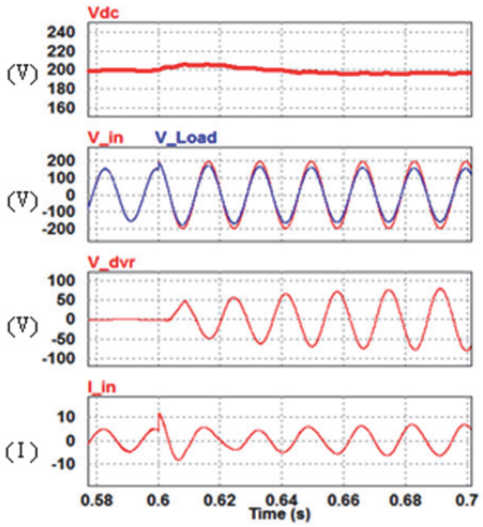

Fig. 8 Voltage swell simulation result (V_{in_rms} = 140 V, load = 363W).

3.1.2 Case 2: DVR reactive current compensation control

Figures 9 and 10 illustrate the performance of reactive current compensation control with DVR's grid-connected inverter. In order to make the reactive current compensation more obvious, the case was tested without load and voltage variations. This function could also be performed with a heavy reactive load condition. Under such a condition, some of the required reactive current was provided by the grid-connected inverter, reducing the overall load current on the power line.

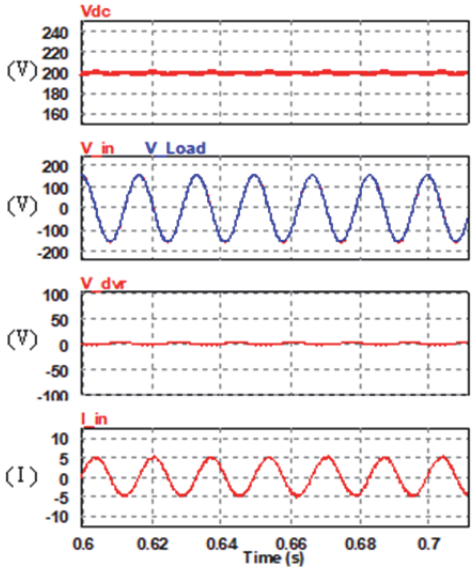

Fig. 9 DVR reactive current (inductive current) control results.

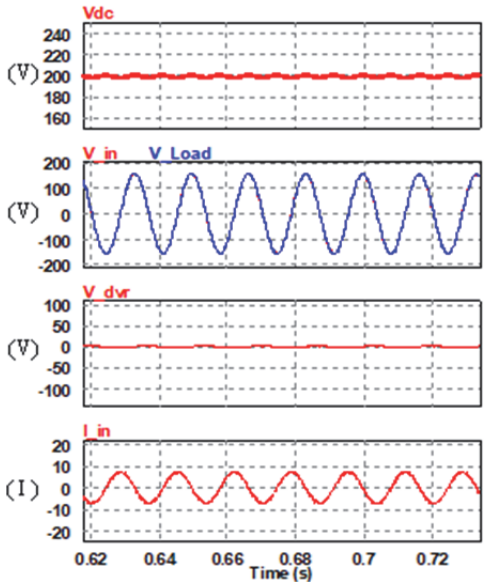

Fig. 10 DVR reactive current (capacitive current) control results.

3.2 Experimental results

In order to verify the performance of the proposed DVR, a 1kVA digitally controlled single-phase back-to-back DVR prototype was developed. The system parameters and operating conditions were the same as those of the simulation cases, and the switching frequency of the inverter was 30 kHz. Figure 11 de-

picts a photograph of the prototype and implementation environment of the proposed DVR experimental circuit. Figures 12-17 show waveforms of the voltage sag/swell compensation and simultaneous reactive power and voltage sag/swell compensation. Figure 12 shows the system parameters in normal state. Figures 13 and 14 illustrate measured voltage waveforms of the dc bus, grid, load and the DVR's output during a voltage sag and swell, respectively. Figures 15 and 16 show the results of DVR performing capacitive (–Q) and inductive (+Q) current regulation of the DVR's shunt inverter with voltage sag and well compensating conditions, respectively. Figure 17 shows the result of the two simultaneously performed control tasks, *i.e.* voltage sag and total load power compensations.

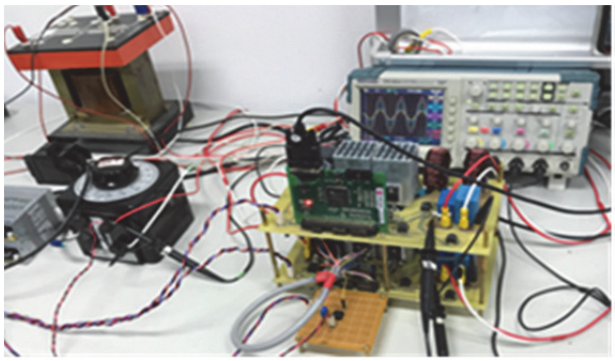

Fig. 11 DVR hardware prototype and implementation environment.

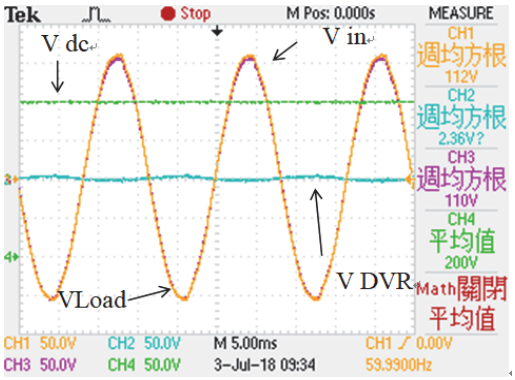

Fig. 12 Waveforms of V_{dc}, V_{in}, V_{Load}, and V_{DVR} under normal system voltage and no compensation (load = 365W).

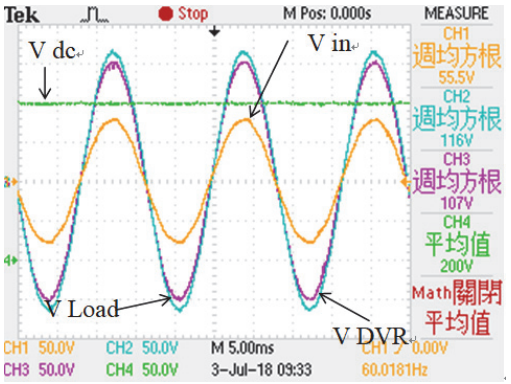

Fig. 13 Waveforms of V_{dc}, V_{in}, V_{Load}, and V_{DVR} during voltage sag (V_{in_rms} = 80 V, load = 363W).

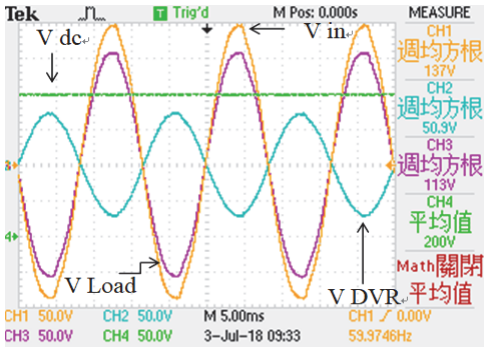

Fig. 14 Waveforms of V_{dc}, V_{in}, V_{Load}, and V_{DVR} during voltage swell (V_{in_rms} = 140 V, load = 363W).

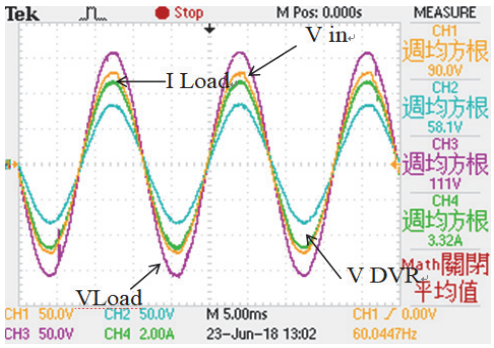

Fig. 15 Waveforms of I_{Load}, V_{in}, V_{Load}, and V_{DVR} during voltage sag (V_{in_rms} = 90 V, load = 363W, Q = 300 Var).

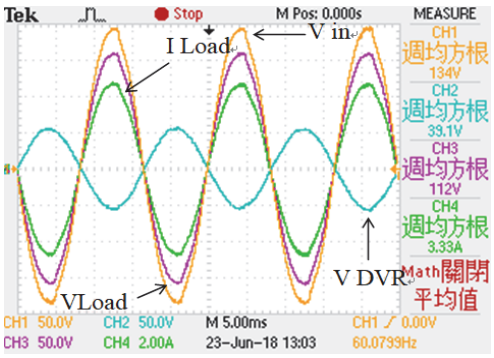

Fig. 16 Waveforms of I_{Load}, V_{in}, V_{Load}, and V_{DVR} during voltage swell (V_{in_rms} = 135 V, load = 363W, Q = –300 Var).

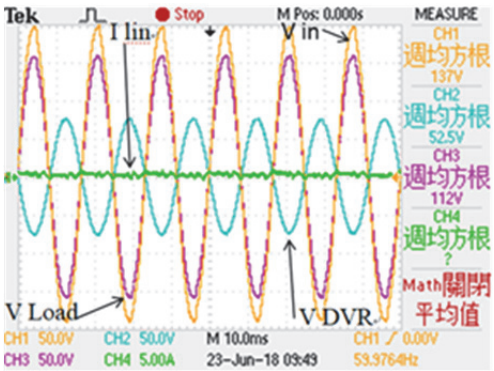

Fig. 17 Waveforms of I_{in}, V_{in}, V_{Load}, and V_{DVR} during voltage swell (V_{in_rms} = 135 V, the load current is completely compensated by the DVR, I_{in} = 0).

4. CONCLUSIONS

Active power distribution systems with various renewable power generations suggest complex power quality problems, especially when it comes to the addition of a large number of harmonic loads. Among the power quality problems, voltage sags and swells appear to have the highest probability of occurrence and a very negative impact on sensitive loads, and thus there is an urgent need to develop appropriate compensation devices and explore appropriate control strategies. In this paper, we have discussed a single-phase back-to-back DVR configuration and the required control scheme for compensating voltage sags and swells without the need for energy storage components. The operation principles of the proposed back-to-back DVR and the related controller design methods have also been discussed in this paper. The simulation studies and hardware tests of the proposed DVR were carried out in several control cases with a 1kVA small-scale hardware prototype. Both simulation and test results verified the effectiveness of the proposed multifunctional back-to-back DVR and related control schemes.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Science and Technology (MOST) of Taiwan for financially support this study regarding power quality control and energy related researches. Grant numbers: MOST Taiwan: MOST 108-2221-E-239-007, MOST 109-2221-E-239-007.

REFERENCES

Ali, K.K., Talei, M., Siadatan, A., and Rad, S.M.H. (2017). "Power quality improvement using novel dynamic voltage restorer based on power electronic transformer." *2017 IEEE Electrical Power and Energy Conference (EPEC)*, Saskatoon, SK, Canada, pp. 1-6

Ali, M.T., Jianhua, Z., Yaqoob, M., Abbas, F., and Rafique, S.F. (2014). "Design of an efficient dynamic voltage restorer for compensating voltage sags, swells, and phase jumps." *2014 16th International Power Electronics and Motion Control Conference and Exposition*, Antalya, Turkey, pp. 1122-1127

Ansal, V., Ravikumar, K., and Parthiban, P. (2016). "Transformerless dynamic voltage restorer for voltage sag mitigation." *2016 Biennial International Conference on Power and Energy Systems: Towards Sustainable Energy (PESTSE)*, Bangalore, India, pp. 1-4

Farhadi-Kangarlu, M., Babaei, E., and Blaabjerg, F. (2017). "A comprehensive review of dynamic voltage restorers." *International Journal of Electrical Power & Energy Systems*, **92**, 136-155

İnci, M., Büyük, M., Tan, A., Bayındır, K.C., and Tümay, M. (2017). "Survey of inverter topologies implemented in dynamic voltage restorers." *2017 4th International Conference on Control, Decision and Information Technologies (CoDIT)*, Barcelona, Spain, pp. 1141-1146

Johnson, D.O. and Hassan, K.A. (2016). "Issues of Power Quality in Electrical Systems." *International Journal of Energy and Power Engineering*, **5**(4), 148-154

Li, P., Holliday, D., and Williams, B.W. (2016). "AC voltage sag-swell compensator based on unified non-inverting and inverting output voltage ac chopper." *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, Glasgow, UK, pp. 1-6

Messiha, M.A., Baraket, C.F., Massoud, A.M., Iqbal, A. and Soliman, R. (2016). "Voltage sag mitigation employing dynamic voltage restorer with minimum energy requirements: Analysis and implementation." *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, Glasgow, UK, pp. 1-6

Ndirangu, J.G., Nderu, J.N., Muhia, A.M., and Maina, C.M. (2018). "Power quality challenges and mitigation measures in grid integration of wind energy conversion systems." *2018 IEEE International Energy Conference (ENERGYCON)*, Limassol, Cyprus, pp. 1-6

Udayakiran, C. and Vali, H. (2017). "Design of battery energy storage system (BESS) support dynamic voltage restorer (DVR) to reduce the rating of voltage source converter (VSC) applied to IEEE 11, 33 & 69 bus systems." *2017 IEEE 7th International Advance Computing Conference (IACC)*, Hyderabad, India, pp. 477-481

Yada, H.K. and Murthy, M.S.R. (2016). "Operation and control of single-phase DVR based on SOGI-PLL." *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, pp. 1-5

Yada, H.K. and Murthy, M.S.R. (2016). "Operation and control of single-phase UPQC based on SOGI-PLL." *2016 7th India International Conference on Power Electronics (IICPE)*, Patiala, India, pp. 1-6.