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An Interleaved High-Step-Up Converter with Improved Voltage Gain and Leakage Inductance Energy Recycled

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ABSTRACT

An interleaved high-step-up converter with voltage gain and improved leakage inductance energy recycling is presented. The tested device achieves a higher voltage gain by use of coupled inductors and energy-transferring capacitors. Implementation of non-floating switches means that no isolated drivers are required. The operating principle and an analysis of the converter are provided and a prototype was built and tested using a 38V input voltage and 400V output voltage, to validate the actual effectiveness of the project.

Keywords: Coupled inductor, Energy-transferring capacitor, High-step-up converter.

1. INTRODUCTION

With global increases in the number and type of electronic devices, and with rapid developments in science and technology, energy demands continue to grow. To facilitate sustainable activities and develop a more environmentally sustainable projects renewable energy sources are now under intensive development. While they may be initially costly to implement, compared to existing means, solar energy, wind power generators, fuel cells, and so on provide great long term potential (Li *et al*. 2009; Li *et al*. 2009; Boico *et al*. 2007). Solar power generation systems and DC-DC converters are of particular interest to researchers because many renewable energy systems, solar included, have a relatively low or unstable output voltage. One means to correct this issue is to install a high boost converter. Conventional boost converters and buck-boost converters are used because of their small component count, simple structure, and low cost. However, since the maximum voltage gain of these devices are limited by their parasitic elements, the voltage gain drops sharply when the duty cycle approaches one (Lin *et al*. 2013), thus it is difficult for them to achieve a high level voltage boost.

Electronic engineering literature is now replete with voltage-boosting converters, and it is necessary to undertake a brief review of what has been done so far. Existing converters typically fall into several categories, energy-transferring capacitors (Liang et al. 2013; Tseng *et al*. 2015; Park *et al*. 2011; Silveira *et al*. 2014), coupled inductors (Liang *et al*. 2013; Tseng *et al*. 2015; Park *et al*. 2011; Silveira *et al*. 2014; Young *et al*. 2014; Tang *et al*. 2015), voltage doubler circuits (Young *et al*. 2014; Tang *et al*. 2015), interleaved circuits (Gules *et al*. 2003; Li and He 2011; Li *et al*. 2012; Dwari and Parsa 2011; Zheng *et al*. 2019; Lai *et al*. 2012; Pan and Lai 2010; Hosseini *et al*. 2014; Tseng and Huang 2014; Tseng *et al*. 2015; Hu and Gong 2015; Pan *et al*. 2014; Pan *et al*. 2013; Pan *et al*. 2016) and more. However, in (Liang *et al*. 2013; Tseng *et al*. 2015; Park *et al*. 2011; Silveira *et al*. 2014; Young *et al*. 2014; Tang *et al*. 2015; Gules *et al*. 2003; Li and He 2011; Li *et al*. 2012), in order to achieve a high voltage gain, applying too many charge pump capacitors to switches and inductors was shown to lead to overly complex structures and generally reduce converter reliability. As shown in other research (Liang *et al*. 2013), the capacitor module, along with the coupled inductor, not only achieves a high voltage boost, but also has a low voltage stress on the switch, reducing losses. Tseng *et al*. 2015, Park *et al*. 2011, and Silveira *et al*. 2014 showed that by superimposing more than two energy-transferring capacitors to achieve high voltage gain, the type of converter used needs to connect an output capacitor to reduce output ripple. Further, literature on voltage doublers (Young *et al*. 2014; Tang *et al*. 2015) showed that the required voltage can be realized by a circuit composed of a plurality of capacitors and diodes. The traditional approach to doubling piezoelectricity is shown in (Young *et al*. 2014), which increases the capacitance and the diode to achieve a high boosting effect. As shown in (Tang *et al*. 2015), the combination of inductor and diode can also be used to double a voltage. This method makes the voltage doubler circuit more flexible in its application.

Other studies (Gules *et al*. 2003; Li and He 2011; Li *et al*. 2012; Dwari and Parsa 2011; Zheng *et al*. 2019; Lai *et al*. 2012; Pan and Lai 2010; Hosseini *et al*. 2014; Tseng and Huang 2014; Tseng *et al*. 2015; Hu and Gong 2015; Pan *et al*. 2014; Pan *et al*. 2013; Pan *et al*. 2016) showed that two or more identical circuits can be applied to an interleaved converter to generate a high boost. This type of converter has the advantage of reducing the component current stress, but with the attendant cost of increasing the number of components used. The converter used in (Gules *et al*. 2003) is composed of two conventional boost converters, two capacitors and two diodes. Whereas, (Li and He 2011; Li *et al*. 2012) used the inductive coupling of two conventional boost converters to reduce the conduction loss of the diode, improving overall efficiency. Other papers such as (Dwari and Parsa 2011) used a coupled inductor to reduce voltage surges caused by the body diode of the switch when the switch is turned off, which aided in energy recovery from the leakage inductance. As shown in (Zheng *et al*. 2019), several energy-transferring capacitors can be added to the circuit topology to give a converter improved voltage gains. Another high-boost circuit with an interleaved architecture

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was proposed in (Lai *et al*. 2012), but the switching duty cycle of this converter had to be above 50%. A modified version of this idea was shown in (Lai *et al*. 2012) and (Pan and Lai 2010), by the addition of a coupled inductor in the converter; this reduced the voltage across the active switch, thereby reducing switching losses. Other researchers (Hosseini *et al*. 2014) demonstrated a high boost by interleaving two coupled inductors. However, in as demonstrated in (Tseng and Huang 2014; Tseng *et al.* 2015; Hu and Gong 2015), the apparent disadvantages of the large number of components becomes apparent; in this case two coupled inductors were applied to the interleaved converter and cooperated with the superimposed output capacitors to achieve a high voltage gain. The paper by (Pan *et al*. 2014) shows a modified version of (Lai *et al*. 2012) with a higher voltage gain than the original; however Pan continued the work (Pan *et al*. 2013; Pan *et al*. 2016) by using a parallel circuit topology involving four conventional boost converters. Although this circuit was able to withstand a higher input current, the efficiency was limited by the excessive number of components.

Despite this slew of research interest, this paper proposes another solution. This design includes an interleaved high-boost converter, with leakage inductance energy recycled, and with an improved voltage gain compared to the circuit demonstrated by (Gules *et al*. 2003). This design derives the high voltage gain from its coupled inductor and energy-transference capacitor. The converter has the following characteristics: (1) Leakage inductance energy can be recovered. There is no clamp circuit, making the device simple; (2) The main switches used share a common ground, removing the need to use an isolated drive circuit; (3) The coupled inductor has both transformer and inductor behavior, which means that the voltage across the energy-transferring capacitor can be improved by adjusting the turns ratio. As with the input inductor of a conventional boost converter, the magnetizing inductance can be used as a voltage-boosting inductor; and (4) The input current ripple of the converter can be reduced, so a capacitor with a lower capacitance value can be used.

2. CIRCUIT DESCRIPTION

Figure 1 shows the architecture of the new high-boost converter proposed herein. This architecture features input current sharing and leakage inductance energy recovery, reducing any voltage surge on the active switch. Additionally, due to the interleave circuit, the phase difference between the two phases is 180 degrees, which reduces input current ripple and output voltage ripple. The converter consists of two active switches S_1, S_2, two coupled inductors N_{p1}, N_{s1} and N_{p2}, N_{s2}, two energy-transferring capacitors C_1, C_2, four diodes D_1, D_2, D_3, D_4, and one output capacitor C_o. The dotted terminals of the primary windings N_{p1} and N_{p2} are both connected to the positive terminal of the input voltage, and the non-dotted terminals of the primary side windings N_{p1} and N_{p2} are connected to the dotted terminals of the secondary windings, N_{s1} and N_{s2}, respectively. These are also connected to the individual switches and capacitors S_1 and C_2, and S_2 and C_1. Input voltage is at V_{in}, output voltage is V_o, and output resistance is R_o.

3. CIRCUIT OPERATING PRINCIPLES

Figure 2 shows an equivalent circuit diagram of the proposed converter. The two coupled inductors are composed of two ideal

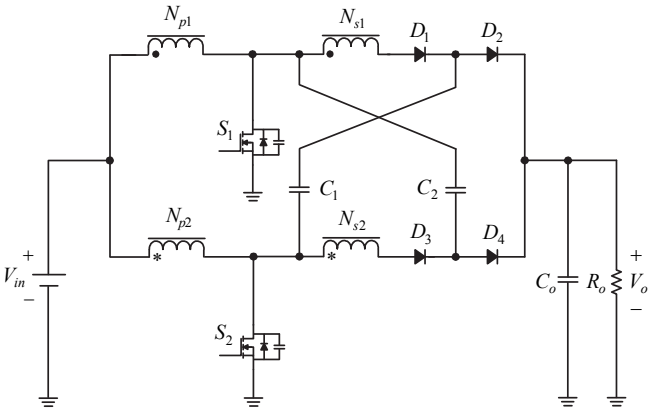


Fig. 1 Schematic diagram of the proposed converter.

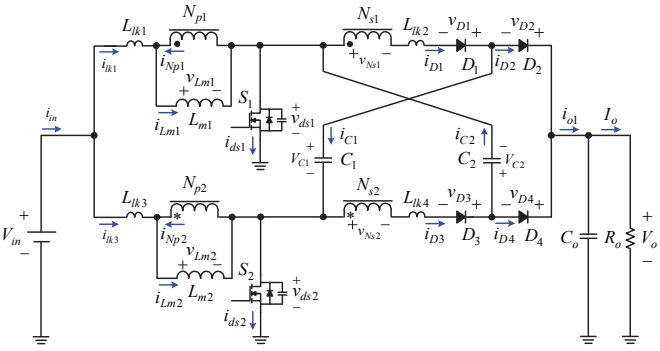


Fig. 2 Equivalent schematic diagram of the proposed converter.

transformers which have primary-side windings N_{p1}, N_{p2}, and secondary side-windings N_{s1}, N_{s2}. The magnetizing inductances L_{m1}, L_{m2} are connected in parallel with the primary-side windings N_{p1} and N_{p2}, respectively; and the four leakage inductances L_{lk1}, L_{lk2}, L_{lk3}, L_{lk4}. In order to simplify this analysis the following assumptions are made:

(1) Assume that the converter operates in CCM.
(2) All diodes and switches except for parasitic diodes and capacitors are assumed to be ideal components.
(3) All capacitances are large enough to keep their voltages at certain values.
(4) The two turns-ratio are identical, that is, $n = N_{s1}/N_{p1} = N_{s2}/N_{p2}$.
(5) T_s is the switching period.

The current flow description for each operating state is included in the following analysis and the associated symbols are thus defined: (i) Input current is expressed by i_{in}, where the currents flowing through N_{p1}, L_{m1}, L_{lk1}, and N_{s1} are indicated by i_{Np1}, i_{Lm1}, i_{lk1}, and i_{D1}, respectively; currents flowing through N_{p2}, L_{m2}, L_{lk3}, and N_{s2} are represented by i_{Np2}, i_{Lm2}, i_{lk3}, and i_{D3}, respectively; currents flowing through S_1, S_2, D_2, D_4, C_1, C_2, and R_o are represented by i_{ds1}, i_{ds2}, i_{D2}, i_{D4}, i_{C1}, i_{C2}, and I_o, respectively; (ii) The voltages across the primary windings N_{p1} and N_{p2} are v_{Lm1} and v_{Lm2}, respectively; voltages across the secondary windings N_{s1} and N_{s2} are v_{Ns1} and v_{Ns2}, respectively; the voltages across the switches S_1 and S_2 are v_{ds1} and v_{ds2}, respectively; the voltages across D_1, D_2, D_3, and D_4 are v_{D1}, v_{D2}, v_{D3}, and v_{D4}, respectively; the voltages across the energy-transferring capacitors C_1 and C_2 are V_{C1} and V_{C2}, respectively; and the voltage across the output capacitor C_o is V_o.

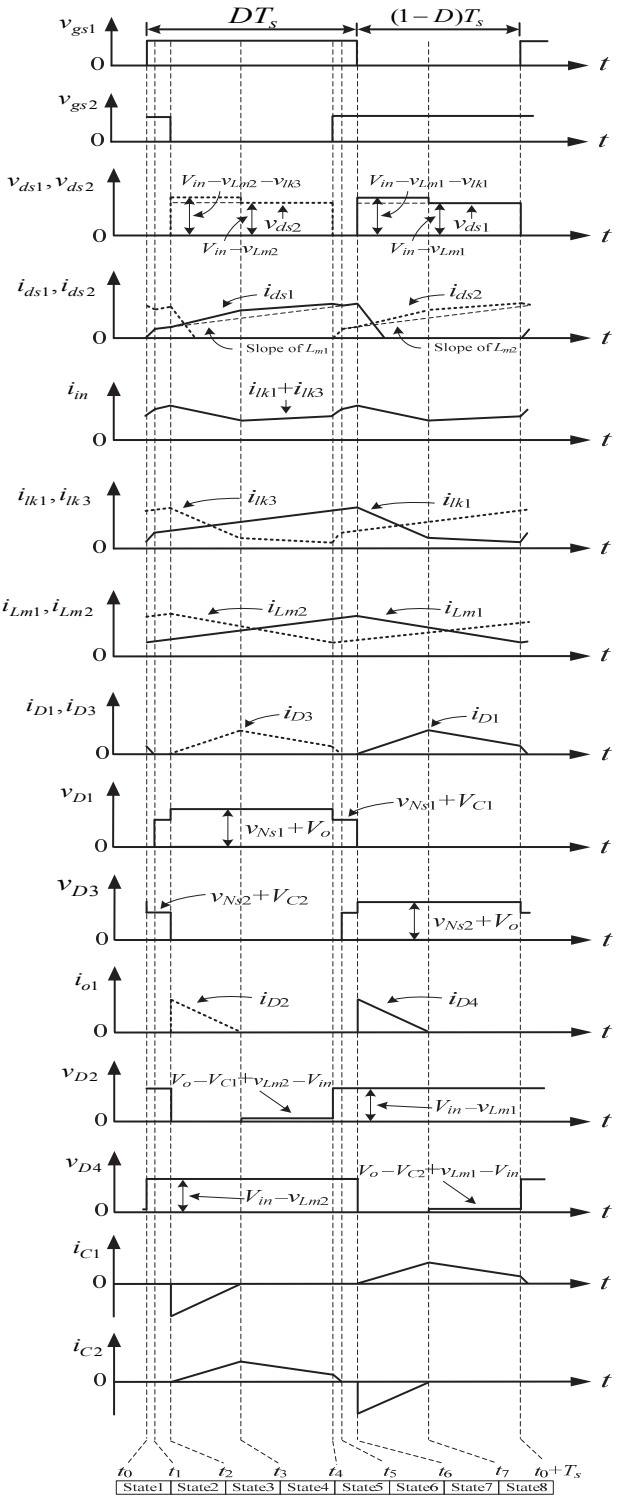
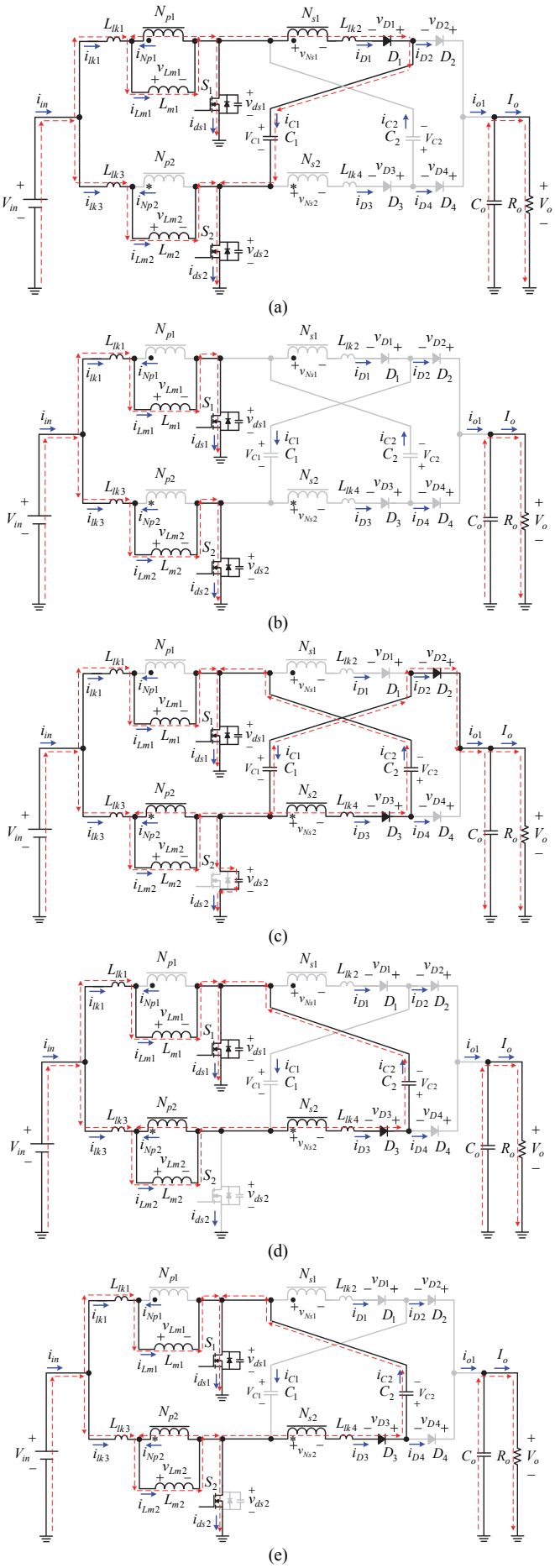


Fig. 3 Key waveforms relevant to the proposed converter operating over one switching period.



Because this converter operates in CCM, there are a total of eight operating states in each switching period. Furthermore, as this architecture is interleaved, there is a symmetric relationship between states one to four, and states five to eight, therefore only a description of states one through four will be offered. Fig. 3 shows the key waveforms of the converter over one full switching period. For convenience of analysis, the voltages across the leakage inductances Llk1, Llk3 will be defined as vlk1, vlk3.

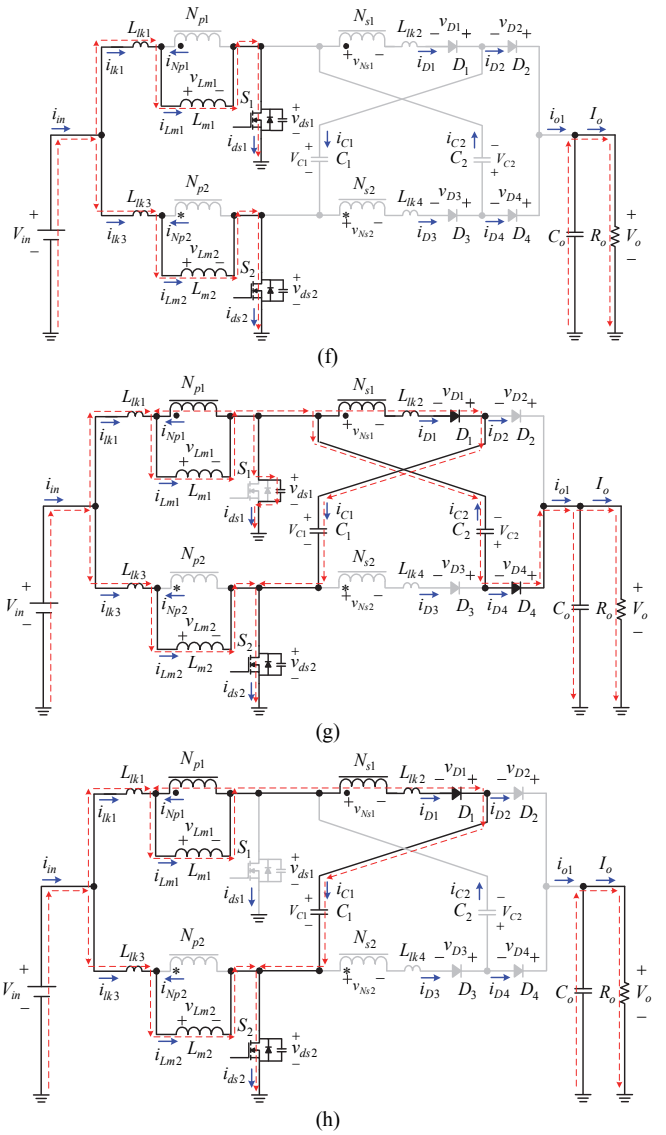


Fig. 4 Operating states over one cycle: (a) state 1; (b) state 2; (c) state 3; (d) state 4; (e) state 5; (f) state 6; (g) state 7; (h) state 8.

3.1 Operating States

State 1: [$t_0 \le t \le t_1$]: As shown in Fig. 4(a), switch *S*1 begins conducting, and switch S_2 is already on. In this interval, the input voltage V_{in} runs across L_{m1}, L_{m2}, L_{lk1}, and L_{lk3}, magnetizing L_{m1}, L_{m2}, L_{lk1} and L_{lk3}. At the same time, due to the demagnetization of the energy stored in the leakage inductance L_{lk2}, the leakage inductance L_{lk2} energy will continue to charge the energy-transferring capacitor C_1. This forces the diode D_1 to continue conducting such that the secondary side-leakage inductance energy can be recovered. Once the energy stored in L_{lk2} is fully released, current i_{D1} drops to zero and this state ends at $t = t_1$. Note that as diode D_2 is reverse-biased, only the output capacitor C_o releases energy to the load.

State 2: [$t_1 \le t \le t_2$]: Following Fig. 4(b), the switches S_1 and S_2 remain on. The input voltage V_{in} still runs across L_{m1}, L_{m2}, L_{lk1} and L_{lk3}, continuing the magnetized state of L_{m1}, L_{m2}, L_{lk1} and L_{lk3}. The energy at leakage inductance L_{lk2} is released entirely. Diode D_1 is reverse-biased and the voltage across it equals V_{D1}. Output capacitor C_o is still releasing energy to the load. This state ends at $t = t_2$.

State 3: [$t_2 \le t \le t_3$]: Fig. 4(c) shows the state where switch S_1 is still active, and switch S_2 starts switching off. In this interval, the input voltage V_{in} still runs across L_{m1} and L_{lk1}, and the inductances L_{m1} and L_{lk1} remain magnetized. Simultaneously, the inductances L_{m2} and L_{lk3} become demagnetized. In this state the second coupled inductor behaves like a transformer, meaning that when the switch is turned off, the coupled inductor releases energy via L_{m2}, as well as transmitting energy via a transferring current, to the secondary side. The input voltage will continue to provide energy to the primary side of the second coupled inductor. Following Kirchhoff's current law, the current i_{lk3} flowing through the leakage inductance L_{lk3} will flow to switch S_2, diode D_2 and diode D_3, namely, $i_{lk3} = i_{ds3} + i_{D2} + i_{D3}$. Since the current i_{D3} flowing to diode D_3 is transferring the current of the second coupled inductor, the energy-transferring capacitor C_2 will charge. Therefore, the switch S_1 will suffer from additional current stress. In addition, part of i_{lk3} flows to the body capacitor of the switch S_2, causing the voltage across the switch S_2 to be $V_{in} - v_{Lm2} - v_{lk3}$. The remaining current across i_{lk3} flows to the load, forcing diode D_2 to be forwar$_d$-biased, whereupon the sum of the input voltage energy, magnetizing inductance energy, leakage inductance energy and transferring capacitor energy supply the load energy. This is the method by which recovery of the primary-side inductance leakage can be achieved. Once the energy stored in L_{lk3} is released entirely, the current at i_{ds2} drops to zero ending the state $t = t_3$.

State 4: [$t_3 \le t \le t_4$]: In the case of Fig. 4(d), switch S_1 is still off. Input voltage V_{in} still runs across L_{m1} and L_{lk1}, magnetizing L_{m1} and L_{lk1}. Magnetizing inductance L_{m2} remains demagnetized and the second coupled inductor still behaves like a transformer. Current flows to diode D_3, where $i_{lk3} = i_{D3}$. In this state the energy at the leakage inductance point L_{lk3} has been released entirely, the voltage across switch S_2 is V_{in}-vL_{m2}. Since the energy in the transferring capacitor C_1 is released entirely, diode D_2 is reverse-biased. In addition, the energy-transferring capacitor C_2 continues to charge, such that the switch S_1 continues to withstand additional current stress, and only the output capacitor releases energy to the load. This state ends when $t = t_4$.

As the circuit states 1 to 4 and 5 – 8 are symmetric, where Figs. 4(a) to 4(d) show states 1 – 4 where the switch *S*1 is always ON; but states 5 to 8, shown in Figs. 4(e) to 4(h) are representative of switch S_2 being always ON. Thus, the operating principles for states 5-8 are not described here.

3.2 Voltage Gain

In order to obtain the voltages across the energy-transferring capacitors C_1, C_2 and the voltage gain of the converter, only states 2, 3 and 7 are considered. Leakage inductances L_{lk1}, L_{lk2}, L_{lk3} and Llk4 are disregarded. From state 2, as shown in Fig. 4(b), the voltages v_{Lm1}, v_{Lm2} at the magnetizing inductances Lm1 and L_{m2} can be determined by:

$$v_{Lm1}^{(2)} = V_{in} \tag{1}$$

$$v_{Lm2}^{(2)} = V_{in} \tag{2}$$

From states 3 and 7, the following equation can be obtained:

$$v_{Lm2}^{(3)} = V_{in} + V_{C1} - V_o \tag{3}$$

$$v_{Lm1}^{(7)} = V_{in} + V_{C2} - V_o \tag{4}$$

Since V_{C1} and V_{C2} are unknown parameters, they must be replaced. As they have the same value only V_{C2} will be used for derivation in this description. By applying the volt-second balance to L_{m1}, the following equation can be obtained:

$$\int_0^{T_s} v_{Lm1} dt = V_{in} \times DT_s + (v_{Lm1}^{(7)}) \times (1-D) T_s = 0 \tag{5}$$

Rearranging (5), the following equation is derived:

$$v_{Lm1}^{(7)} = \frac{-D}{1-D} V_{in} \tag{6}$$

Then, in state 3, based on Kirchhoff's voltage law, the voltage across capacitor C_2 is:

$$\begin{aligned} V_{C2} &= V_{in} - n \cdot v_{Lm1}^{(7)} - v_{Lm1}^{(7)} \\ &= V_{in} + n \cdot \frac{D}{1-D} V_{in} + \frac{D}{1-D} V_{in} \\ &= \frac{1-D+nD+D}{1-D} V_{in} \\ &= \frac{1+nD}{1-D} V_{in} \end{aligned} \tag{7}$$

Substituting (7) into (4) yields:

$$v_{Lm1}^{(7)} = V_{in} + \frac{1+nD}{1-D} V_{in} - V_o \tag{8}$$

Given (1) and (8), applying the volt-second balance to magnetizing inductance Lm1 gives:

$$\begin{aligned} &\int_0^{T_s} v_{Lm1} dt = V_{in} \times DT_s \\ &+ \left(V_{in} + \frac{1+nD}{1-D} V_{in} - V_o \right) \times (1-D) T_s = 0 \end{aligned} \tag{9}$$

After rearranging the above equation, the voltage gain of this converter can be obtained by the following:

$$\frac{V_o}{V_{in}} = \frac{2+nD}{1-D} \tag{10}$$

where

$$n = \frac{N_{s1}}{N_{p1}} = \frac{N_{s2}}{N_{p2}} \tag{11}$$

Following the derivation of (10), given different turns-ratios, curves for the voltage gain can be plotted against duty cycles, as in Fig. 5.

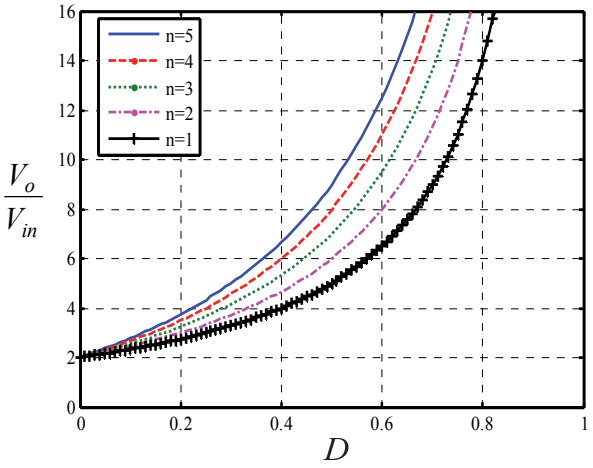


Fig. 5 Curves of voltage gain versus duty cycle for the proposed circuit.

3.3 Boundary conditions of the magnetizing inductance

Conditions required for the converter to operate are:

$$\begin{cases} 2I_{Lm1} \geq \Delta i_{Lm1}, \text{CCM} \\ 2I_{Lm1} < \Delta i_{Lm1}, \text{DCM} \end{cases} \tag{12}$$

where I_{Lm1} and Δi_{Lm1} are DC components and AC components, respectively.

For convenience of analysis, only the magnetizing inductance L_{m1} will be analyzed here. Input power is assumed to be equal to output power. Given that the volt-seconds balance and the ampere-seconds balance, DC voltage on the magnetizing inductance and DC currents at C_1, C_2 and C_o are all zero; therefore, in Figs. 6 and 7, the DC component at i_{Ns1} (I_{Ns1}) is equal to the DC current I_{D1} flowing through diode D_1, or the output current Io. Also, according to Kirchhoff's current law, the DC component at i_{Lm} (I_{Lm1},) is equal to the value of the DC component of the current i_{Np1} (I_{Np1}), plus half of the DC component i_{in} (I_{in}.). Therefore, I_{Lm1} can be described mathematically by the following:

$$I_{in} = \frac{2+nD}{1-D} \times I_o \tag{13}$$

$$I_{Np1} = \frac{N_{s1}}{N_{p1}} \times I_{Ns1} = \frac{N_{s1}}{N_{p1}} \times I_{D1} = \frac{N_{s1}}{N_{p1}} \times \frac{I_o}{2} \tag{14}$$

$$\begin{aligned} I_{Lm1} &= 0.5 \times I_{in} + I_{Np1} \\ &= \frac{1}{2} \times \frac{2+nD}{1-D} \times I_o + n \times \frac{I_o}{2} = \frac{2+n}{1-D} \times \frac{I_o}{2} \end{aligned} \tag{15}$$

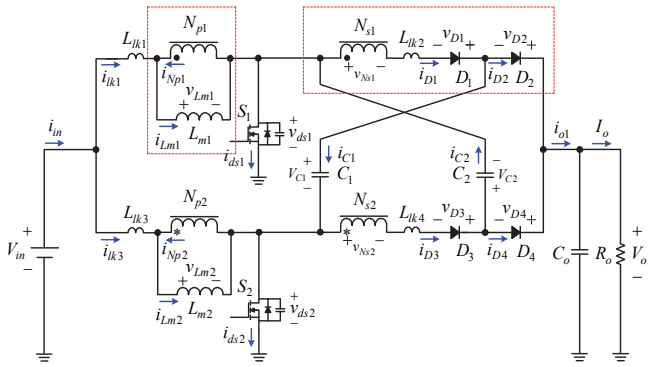


Fig. 6 Labeled area used to explain the I_{Np1} and I_{Lm1} of the proposed converter.

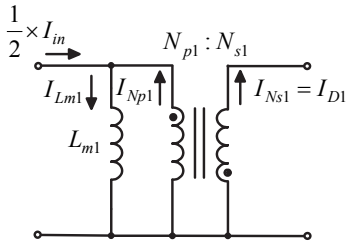


Fig. 7 Equivalent DC analysis of the first coupled inductor.

In Fig. 7, I_o can be expressed as V_o/R_o, which can then be substituted into (15), giving the following relationship:

$$I_{Lm1} = \frac{1}{2} \times \frac{2+n}{1-D} \times \frac{V_o}{R_o} \tag{16}$$

Where the expression of in CCM is

$$\Delta i_{Lm1} = \frac{v_{Np1}\Delta t}{L_{m1}} = \frac{v_{Lm}^{(2)} DT_s}{L_{m1}} = \frac{V_{in}\, DT_s}{L_{m1}} \tag{17}$$

If $2I_{Lm1} \geq \Delta i_{Lm1}$, the magnetizing inductance Lm1 operates in CCM. Substituting (16) and (17) into (12), the following result can be obtained:

$$\begin{aligned} & 2I_{Lm1} \geq \Delta i_{Lm1} \\ & \Rightarrow 2 \times \left(\frac{1}{2} \times \frac{2+n}{1-D} \times \frac{V_o}{R_o} \right) \geq \frac{V_{in}\, DT_s}{L_{m1}} \\ & \Rightarrow \frac{2L_{m1}}{R_o T_s} \geq \frac{2 \times D(1-D)^2}{(2+n)(2+nD)} \\ & \Rightarrow K_1 \geq K_{crit1}(D) \end{aligned} \tag{18}$$

where $K_1 = \dfrac{2L_{m1}}{R_o T_s}$ and $K_{crit1}(D) = \dfrac{2 \times D(1-D)^2}{(2+n)(2+nD)}$.

Equation (18) holds true where the turns-ratio n is equal to 3, and the duty cycle D is changed from zero to 1. As seen from Fig. 8, if K_1 is greater than K_{crit1}, the magnetizing inductor will operate in CCM; otherwise, the magnetizing inductor will operate in DCM.

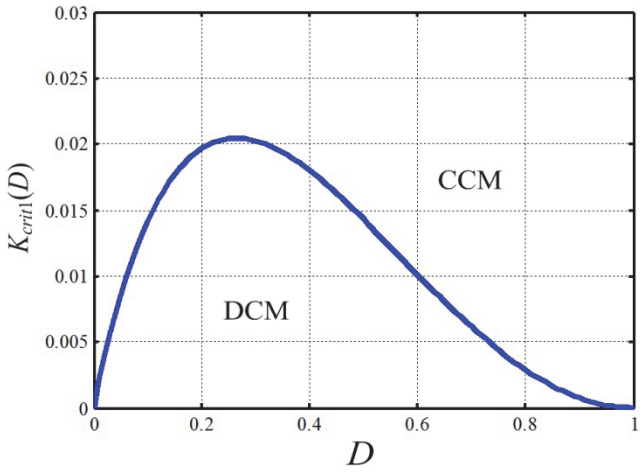


Fig. 8 Boundary conditions for the first magnetizing inductor.

It follows that the procedure for deriving the boundary conditions of the second magnetizing inductor are almost the same as for the first.

4. CONTROL METHODS AND DESIGN CONSIDERATIONS

Figure 9 shows the system block diagram. First, based on the voltage divider, the output voltage is determined, then this value is passed to the analog-to-digital converter (ADC) inside the digital signal processor (DSP). The ADC is used to convert the analog signal to its corresponding digital signal. This digital signal is then sent to the proportional-integral (PI) controller, which is written in the DSP internal interrupt subroutine. This in turn uses an internal enhanced pulse width modulation (EPWM) generator to send out the processed signal, the digital control force signal. Finally, the DSP transmits this digital signal to the switch after the gate driver, to prevent the switch not being fully activated. The relevant system specifications and component names used in the prototype converter are shown in Tables 1 and 5, respectively.

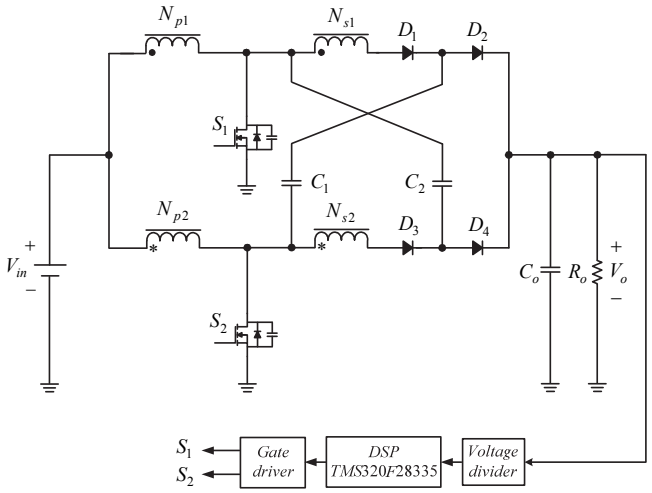


Fig. 9 System block diagram of the proposed converter.

Table 1 System specifications

Specifications	Parameters
Input voltage (V_{in})	38 V
Rated output voltage (V_o)	400 V
Rated output current ($I_{o,\ rated}$)/power ($P_{o,\ rated}$)	1 A / 400 W
Minimum output current ($I_{o,\ min}$) / power ($P_{o,\ min}$)	0.1 A / 40 W
Switching frequency (f_s)	100 kHz

4.1 Design of the Magnetizing Inductance of the First Coupled Inductor

It can be determined from (18) that if the magnetizing inductance of the first coupled inductor is always operating in CCM, the value of the magnetizing inductance L_{m1} must satisfy the following inequality:

$$\begin{aligned} L_{m1} &\geq \frac{2\times D(1-D)^2}{(2+n)(2+nD)}\times\frac{R_{o,max}\,T_s}{2} \\ \Rightarrow L_{m1} &\geq \frac{2\times D(1-D)^2}{(2+n)(2+nD)}\times\frac{V_o}{I_{o\_min}}\times\frac{T_s}{2} \end{aligned} \tag{19}$$

In (19), $R_{o,\ max}$ is the maximum load resistance under light loads, and $I_{o,\ min}$ is the minimum load current under light loads.
By substituting these system specifications into (19), it is possible to derive the value range for L_{m1}:

$$\begin{aligned} L_{m1} &\geq \frac{2\times D(1-D)^2}{(2+n)(2+nD)}\times\frac{V_o}{I_{o\_min}}\times\frac{T_s}{2} \\ \Rightarrow L_{m1} &\geq \frac{2\times 0.63\times(1-0.63)^2}{(2+3)(2+3\times 0.63)}\times\frac{400}{0.1}\times\frac{10\mu}{2} \\ \Rightarrow L_{m1} &\geq 180.51\,\mu\text{H} \end{aligned} \tag{20}$$

In this case, the value of 196.26 μH was selected for L_{m1}, which means it is also the same value for L_{m2}.

4.2 Selection of Coupled Inductor Core

According to Faraday's law, the number of turns of the first coupled inductor's primary winding, N_{p1}, is:

$$N_{p1} = \frac{L_{m1} I_{Lm1\_peak}}{A_e\, B_{max}}\times 10^8 \tag{21}$$

where A_e is the effective cross-sectional area of the core, and B_{max} is the maximum effective magnetic flux density. In addition, as the core rises in temperature, its saturation magnetic flux density (B_s) decreases, making it easier for the core to enter the saturation region, causing short-circuits between components. Therefore, the value of B_{max} is intentionally limited to an 80% threshold of B_s. For this prototype a high-magnetic permeability iron manufactured by TDK Corporation was used (PC47ETD39/20/13-Z), details are listed in Table 2.

Table 2 PC47ETD39/20/13-Z core specifications

Core type	PC47ETD39/20/13-Z
Inductance coefficient (A_L)	3150 ± 25%
Saturation flux density (B_s)	4200 G
Residual magnetic flux density (B_r)	600 G
Effective cross-sectional area (A_e)	1.25 cm^2
Effective volume (V_e)	11.5 cm^3
Magnetic circuit effective length (l_e)	9.21 cm

Substituting the obtained value of L_{m1}, here 196.26 μH, and the specifications listed in Tables 1 and 2 into equation (21), the number of turns on the primary side, N_{p1}, are:

$$\begin{aligned} N_{p1} &= \frac{L_{m1} I_{Lm1\_peak}}{A_e\, B_{max}}\times 10^8 \\ &= \frac{196.26\,\mu\times 7.377}{1.25\times(4200\times 0.8)}\times 10^8 = 34.47\ \text{Turns} \end{aligned} \tag{22}$$

Therefore the value for N_{p1} is 35, and the number of turns on the secondary side, N_{s1}, is 105, since the turns-ratio $n = 3$.

4.3 Air Gap of the Used Core

With the value of N_{p1} selected and the inductance coefficient A_L of the selected core substituted into (23), the value of the corresponding magnetizing inductance $\tilde{L}_{m1}$ can be obtained. This value is much greater than was required for the design:

$$\tilde{L}_{m1} = N_{p1}^2 \times A_L = 35^2 \times 3150\times 10^{-9} = 3.859\,\text{mH} \tag{23}$$

Therefore, an air gap l_a must be inserted into the core to tune A_L to the desired value. First, the required inductance coefficient is calculated:

$$\tilde{A}_L = \frac{L_{m1}}{N_{p1}^2} = \frac{196.32\,\mu}{35^2} = 160.261\,\text{nH/N}^2 \tag{24}$$

Followed by the equivalent reluctance, after the air gap is added, $R_{eq} = R_a + R_e$, where R_a is the air-gap reluctance. R_{eq} is expressed by (25), and R_e is expressed by (26).

$$R_{eq} = \frac{1}{\tilde{A}_L} = \frac{1}{160.261\times 10^{-9}} = 6.24\times 10^6\,\text{A}\cdot\text{Turns / Wb} \tag{25}$$

$$R_e = \frac{1}{A_L} = \frac{1}{3150\times 10^{-9}} = 0.317\times 10^6\,\text{A}\cdot\text{Turns / Wb} \tag{26}$$

Hence, the air-gap reluctance R_a can be determined as follows:

$$\begin{aligned} R_{eq} &= R_a + R_e \Rightarrow R_a = R_{eq} - R_e \\ \Rightarrow R_a &= 6.24\times 10^6 - 0.317\times 10^6 \\ \Rightarrow R_a &= 5.923\times 10^6\,\text{A}\cdot\text{Turns / Wb} \end{aligned} \tag{27}$$

By substituting (27) and the core specifications shown in Table 2 into the magnetoresistance equation, the air gap l_a can be derived by:

$$\begin{aligned} l_a &= R_a \times \mu_0 \times \mu_r \times A_e \\ &= 5.923\times 10^6 \times 4\pi \times 10^{-8} \times 1 \times 1.25 \\ &= 0.93\,\text{mm} \end{aligned} \tag{28}$$

Finally, the value of l_a is determined to be about 0.93 mm.

The following section measures the coupled inductor design using an LCR meter at 100 kHz, and results are shown in Tables 3 and 4.

Table 3 Measurements for the first coupled inductor

Number of primary-side turns N_{p2}	35 Turns
Number of secondary-side turns N_{s2}	105 Turns
Primary-side inductance L_{Np1_open} under the secondary-side open circuit	196.42 μH
Primary-side inductance L_{Np1_short} under the secondary-side short circuit	0.45 μH
Secondary-side inductance L_{Ns1_open} under the primary side open circuit	1.84 mH
Secondary-side inductance L_{Ns1_short} under primary-side short circuit	7.6 μH

Table 4 Measurements for the second coupled inductor

Number of primary-side turns N_{p2}	35 Turns
Number of secondary-side turns N_{s2}	105 Turns
Primary-side inductance L_{Np2_open} under the secondary-side open circuit	198.42 μH
Primary-side inductance L_{Np2_short} under the secondary-side short circuit	0.41 μH
Secondary-side inductance L_{Ns2_open} under the primary side open circuit	1.94 mH
Secondary-side inductance L_{Ns2_short} under primary-side short circuit	8.7 μH

By substituting the values measured in Table 3 into (29), the value of the coupling coefficient k, of the primary side to the secondary side, can be obtained:

$$k_1 = \sqrt{1 - \frac{L_{Np1\_short}}{L_{Np1\_open}}} \cong 0.99885 \tag{29}$$

By substituting the values measured in Table 3 into (30), the value of the coupling coefficient k with the secondary side relative to the primary side can be obtained:

$$k_2 = \sqrt{1 - \frac{L_{Ns1\_short}}{L_{Ns1\_open}}} \cong 0.99793 \tag{30}$$

By substituting the results of (29) and (30) into the geometric mean equation, the common coupling coefficient kcomm can be obtained:

$$k_{comm} = \sqrt{k_1 k_2} \cong 0.99839 \tag{31}$$

Then, the obtained kcomm and some measured values in Table 3 are substituted into equations (32) and (33). From this the primary leakage inductance L_{lk1} and secondary leakage inductance L_{lk2} of the first coupled inductor can be obtained:

$$\begin{aligned} L_{lk1} &= (1 - k_{comm}) L_{Np1\_open} \\ &= (1 - 0.99839) \times 196.42\mu = 0.316\ \mu\text{H} \end{aligned} \tag{32}$$

$$\begin{aligned} L_{lk2} &= (1 - k_{comm}) L_{Ns1\_open} \\ &= (1 - 0.99839) \times 1.84\,\text{m} = 2.96\ \mu\text{H} \end{aligned} \tag{33}$$

Therefore, the values of L_{lk1} and L_{lk2} are 0.316 μH and 2.96 μH, respectively. By the same way, the values of L_{lk3} and L_{lk4} are 0.331 μH and 3.156 μH.

4.4 Design of Energy-Transferring Capacitor C_1 and C_2

As a result of the above analysis, it can be seen that capacitor C_2 does not operate when switch S_1 is on, and it is only charged/discharged in the interval when switch S_1 is off. In the interval D_a, capacitor C_2 continues to discharge until the energy release is completed, so that the current i_{C2} rises from the negative current to the zero current. Therefore, the width of the duty cycle when current i_{C2} rises from the negative to zero, can be found by the slope equation $y = ax + b$. This width can be expressed as follows:

$$D_a = 0.136 \tag{34}$$

Therefore, the constant value $I_{C2(Da)}$, corresponding to the current i_{C2} during the discharge period, can be obtained by:

$$I_{C2(Da)} = \frac{I_{Lm1\_peak}}{2} = \frac{7.377}{2} = 3.689\text{A} \tag{35}$$

Also, since Tables 1 and 5 show the voltage stresses on C_1 and C_2 are the same, here referred to as V_{C1} and V_{C2}, respectively, V_{C1} and V_{C2} can be calculated by:

$$\begin{aligned} V_{C1} = V_{C2} &= \frac{1 + nD}{1 - D} V_{in} \\ &= \frac{1 + 3 \times 0.63}{1 - 0.63} \times 38 \\ &= 296.81\text{V} \end{aligned} \tag{36}$$

Based on (34), (35), (36) and Tables 1 and 5, the maximum voltage ripple on C_2 is set within 0.1% of V_{C2}, thus the value of C_2 is:

$$C_2 \geq \frac{I_{C2(Da)}\, D_a\, T_s}{\Delta v_{C2}}$$

$$\Rightarrow C_2 \geq \frac{0.136 \times 3.689 \times 10\,\mu}{2 \times 0.001 \times 296.81} = 8.452\ \mu\text{F} \tag{37}$$

Hence, one 22 μF/450V Rubycon electrolytic capacitor is used for C_2, and also for C_1.

Table 5 components used in the converter

Component	Specification
MOSFET switch S_1, S_2	IRFB4227PBF
Diode D_1, D_3	ISL9R860P2
D_2, D_4	GMR10H200C
Capacitor C_1, C_2	22 μF/450V
Output capacitor	C_o 180 μF/450V
Coupled Inductor 1	Core: ETD39/20/13-Z n = 3, L_{m1} = 196.26 μH, L_{lk1} = 0.32 μH, L_{lk2} = 2.96 μH
Coupled Inductor 2	Core: ETD39/20/13-Z n = 3, L_{m1} = 196.26 μH, L_{lk3} = 0.33 μH, L_{lk4} = 3.16 μH, L_{m2}= 198.42 μH

5. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed converter, the waveforms from Figs. 10 to 19 were measured under the rated load conditions.

As seen from Fig. 10, there is a voltage surge across the v_{ds1} and v_{ds2} on the main switches S_1 and S_2. The main reason for this is that when the main switches S_1 and S_2 are turned off, the primary-side leakage inductances L_{lk1} and L_{lk3} of the two coupled inductors transfer energy to the load through the energy-transferring capacitors C_1 and C_2, respectively. In addition, if the energy stored in C_1 and C_2 has fully discharged, but the primary-side leakage inductance energy has not, then the remaining energy in the primary-side leakage inductance charges at C_1 and C_2 through the diodes D_1 and D_2, respectively. This is the aspect of the design that enables energy leakage recovery. Thus, voltage surges on the main switches S_1 and S_2 can also be reduced. Note, however, that as load increases, increases in the energy stored in the primary-side leakage inductance will cause a portion of the leakage inductance energy to charge the parasitic capacitance of the main switch, causing a high-frequency oscillating voltage on the switch.

As seen from Fig. 11, the currents i_{ds1} (or i_{ds2}) flowing through the main switches S_1 (or S_2) have high-frequency current oscillations. The main reason for this is that when both main switches are turned on in state 1 (or 5), the energy stored in the secondary-side leakage inductance L_{lk2} (or L_{lk4}) will be released. Whereupon the energy-release path leads to the main switches S_1 and S_2. Therefore, at this time, the leakage inductance can be connected in series with the energy- transfer capacitor C_1 (or C_2) generating a high-frequency oscillating current. When the energy stored in the leakage inductance reaches zero, diode D_1 (or D_3) create a reverse recovery current. Therefore, at this time, the leakage inductance L_{lk2} (or L_{lk4}) will oscillate with the energy-transferring capacitor C_1 (or C_2) connected in series with the parasitic capacitance of the diode D_1 (or D_3). By doing so, a high-frequency oscillating current on the primary side of the first (or second) coupled inductor is induced. This current will then flow to the main switch S_1 (or S_2). That is, $i_{ds1} = i_{Lm1}\text{-}i_{Np1}\text{-}i_{D1} = i_{Lm1}\text{-}(n + 1)i_{D1}$, such that the high-frequency oscillating current on the primary side will be $(n + 1)$ times that of the secondary side. On the other hand, when switch $S1$ is on, and switch S_2 is off, the current ids1 flowing through the main switch S_1 is equal to $i_{Lm1} + i_{D3}$, and the current i_{D3} becomes the charging current for C_2. At the same time, current i_{D3} will increase as the load increases, so its proportion as part of the current i_{ds1} gradually increases. This will make the current in the switch appear as a bump, where the current in i_{D3} is the additional current stress that the switch needs to withstand.

As shown in Fig. 12, the primary-side leakage inductance current i_{lk1} of the first coupled inductors, and the primary-side leakage inductance current i_{lk3} of the second coupled inductors, have high-frequency oscillating currents, and at the interval in which the two switches are turned on, these currents are mainly the same as the current flowing through the switches. These are referred to as i_{ds1} and i_{ds2} and they flow through the main switches S_1 and S_2. In state 4, when switch $S1$ is on and switch S_2 is off; or in state 8, when switch S1 is off and switch S_2 is on, the magnetizing inductance L_{m1} (or L_{m2}) is demagnetized and charges the energy-transferring capacitors C_1 or C_2, respectively. Note that the currents i_{Lm1} or i_{Lm2} have $(n + 1)$ times the current of the secondary-side currents i_{D1} or i_{D3}. Thus the currents i_{D1} and i_{D3} will be equal to the leakage inductance currents i_{lk1} and i_{lk3}, respectively. Current i_{lk3} is such that when one switch is turned on and the other off, the primary-side leakage current has a change of $(1 + n)$.

Figure 13 shows that the voltages across V_{D1} at diode D_1, and the voltage across diode D_2, exhibit voltage spikes. This phenomenon arises as a result of the secondary-side leakage inductances L_{lk2} and L_{lk4} as they resonate with the parasitic capacitances of the diodes D_1 and D_2. Additionally, since diode D_1 uses a fast diode with a rated voltage of 600V, its reverse recovery current will be larger than that of the Schottky diode, meaning that the voltage V_{D1} will exhibit a greater voltage spike. Also, diode D_2 exhibits a voltage spike in the cut-off instant, meaning that the remaining voltage oscillations in the cut-off interval are affected by diode D_1. Since diodes D_3, D_4 in Fig. 13 and diodes D_1 and D_2 in Fig. 15 are complementary, the operational principles are the same, therefore no further description is made.

As can be seen from Fig. 14, the current i_{D1} through diode D_1 is a current for charging the energy-transferring capacitor C_1, whereas the current i_{D2} flowing through diode D_2 is a current for discharging the energy-transferring capacitor C_1. The oscillating current generated in the interval where both switches are turned on arises in state 1. When S_1 is turned on and switch S_2 is turned off, the voltage across the energy-transferring capacitor C_2, the input voltage V_{in}, the voltage $-v_{lk3}$, and the voltage across the excitation inductor L_{m2} are all connected in series and supply energy to load. Hence, at this moment, the energy stored in L_{lk3} will be instantaneously released, inducing a current spike at i_{D2}. This spike will also increase as load increases. Since diodes D_3 and D_4 in Figs. 14, and diodes D_1 and D_2 in Fig.16 are complementary, the operational principles are the same, therefore no further description is made.

Figure 17 shows that the voltage across the energy-transferring capacitor C_1 and the voltage across the energy-transferring capacitor C_2 are both stable.

In Fig. 18, current i_{C1} flows through the energy-transferring capacitor C_1, current i_{C2} flows through the energy-transferring capacitor C_2, and the currents i_{D1} and i_{D3} flow through the diodes D_1 and D_3. That is, the currents for charging the energy-transferring capacitors C_1 and C_2, are the currents i_{D1} and i_{D3} flowing through the diodes D_1 and D_3; the currents for discharging the energy-transferring capacitors C_1 and C_2 are the currents i_{D2} and i_{D4} flowing through the diodes D_2 and D_4.

Figure 19 shows the current io1 synthesized by the rising currents i_{D2} and i_{D4} that flow through diodes D_2 and D_4. Note that the period of current $io1$ will be 1/2 that of the switching period, so its frequency will be twice the switching frequency. Therefore, when designing the output capacitor C_o, a smaller output capacitance can be used.

Figure 20 presents a curve of efficiency versus load current. It can be seen that efficiency over the full load range is greater than 91.17%, the rated-load efficiency is about 94.03%, and maximum efficiency can be as high as 94.52%. Fig. 21 is a photograph of the prototype converter.

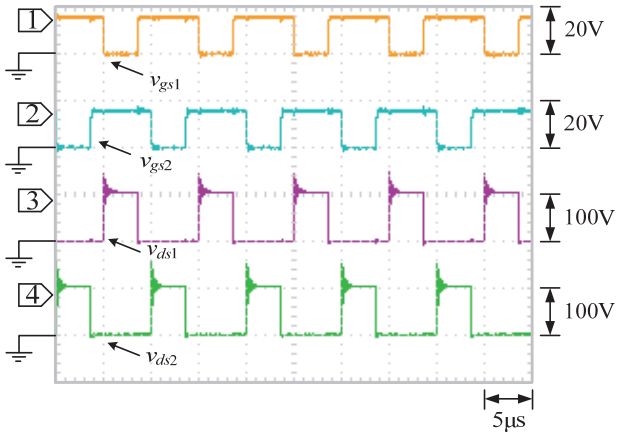


Fig. 10 Measured waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{ds1}; (4) v_{ds2}.

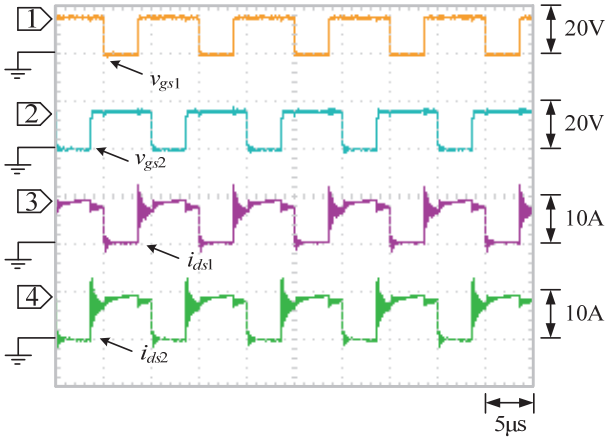


Fig. 11 Measurement waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{ds1}; (4) i_{ds2}.

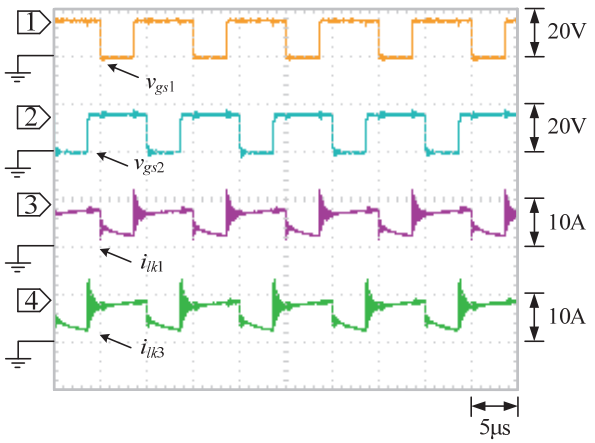


Fig. 12 Measurement waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{lk1}; (4) i_{lk3}.

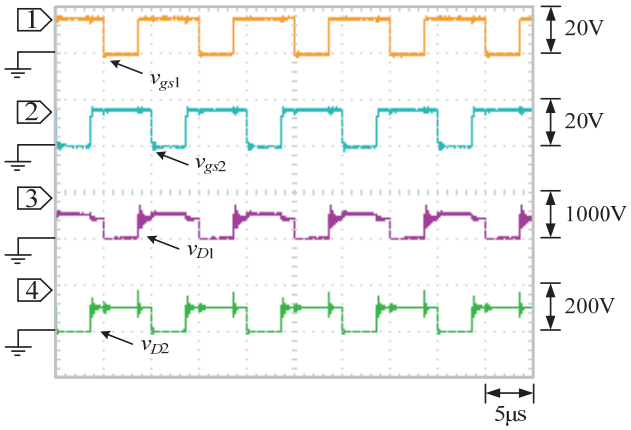


Fig. 13 Measurement waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{D1}; (4) v_{D2}.

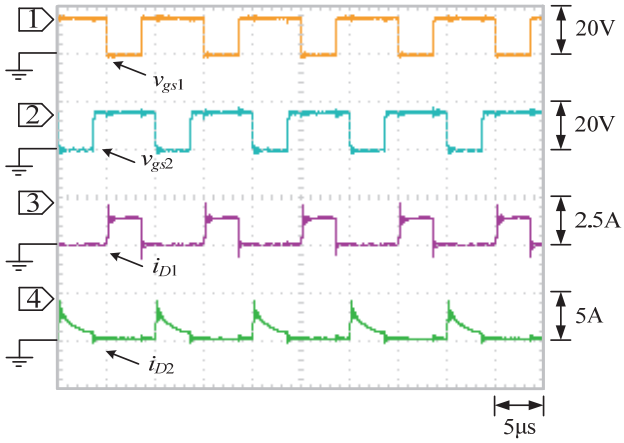


Fig. 14 Measured waveform at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{D1}; (4) i_{D2}.

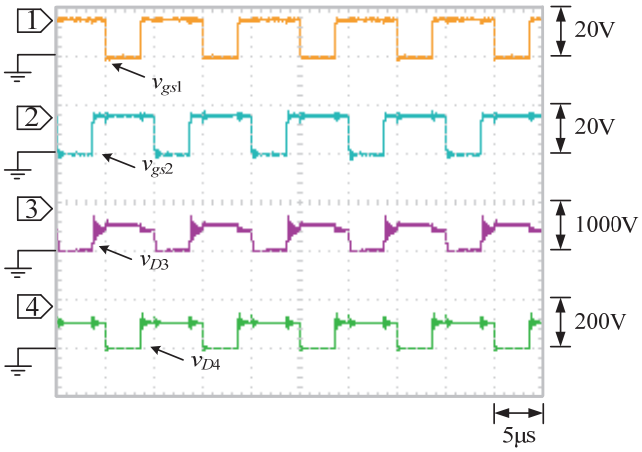


Fig. 15 Measured waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{D3}; (4) v_{D4}.

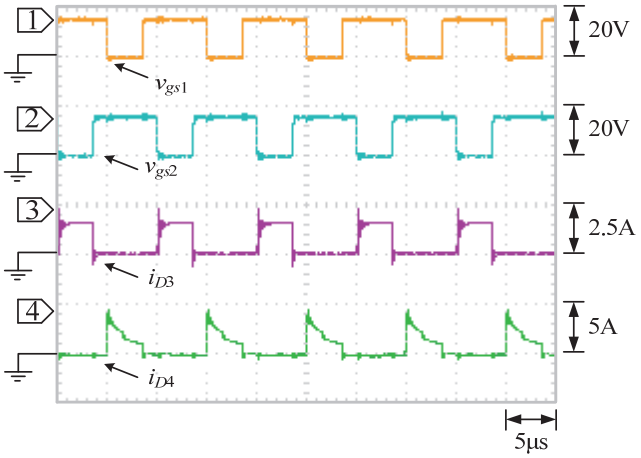


Fig. 16 Measured waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{D3}; (4) i_{D4}.

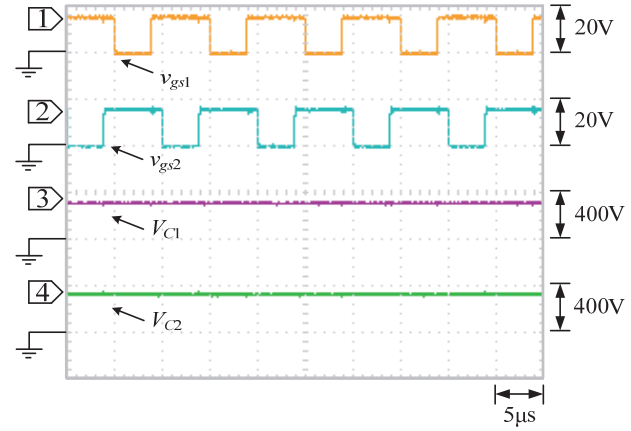


Fig. 17 Measured waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

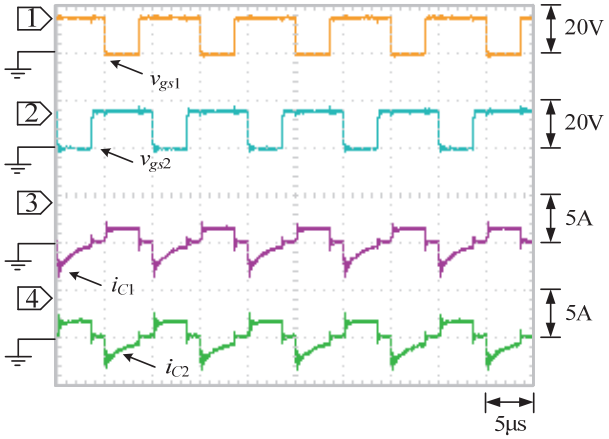


Fig. 18 Measurement waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{C1}; (4) i_{C2}.

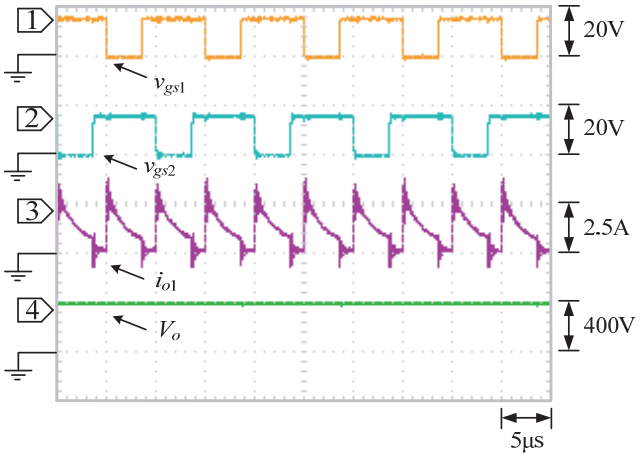


Fig. 19 Measurement waveform at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{o1}; (4) V_o.

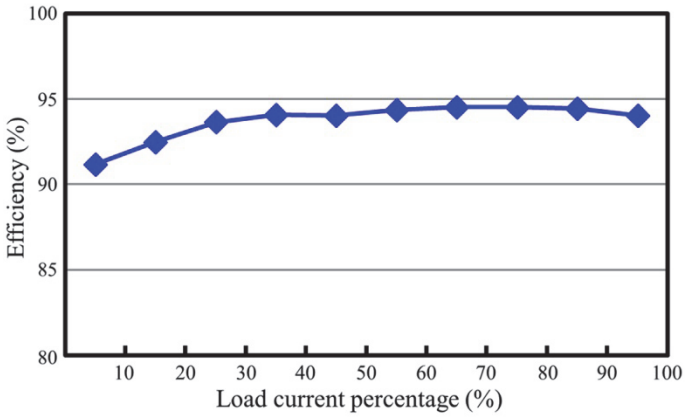


Fig. 20 Curve of efficiency versus load current percentage.

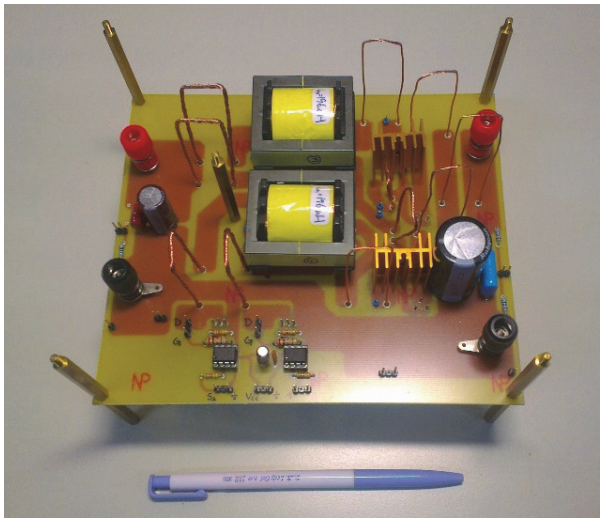


Fig. 21 Photo of the prototype of the proposed circuit.

6. CONCLUSION

This paper proposed and examined an interleaved high-boost converter with improved voltage gain and recovered leakage inductance energy. The voltage gain was derived/obtained using coupled inductors and energy-transferring capacitors that could be adjusted by means of the duty cycle and turns-ratio. The leakage inductance energy of the coupled inductor was made recoverable, such that the voltage spikes on the main switches were quite small. This converter was easy to drive and would be suitable for industrial applications.

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