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An Investigation into a ZVS Resonant Converter to Achieve Wide Voltage Operation

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ABSTRACT

A new zero voltage switching *LLC* resonant converter is presented to have the feature of wide-voltage input operation. The circuit configuration of the presented circuit topology has two converter legs on the input-side to lessen voltage rating on power semiconductors and two secondary windings on low-voltage side to implement wide input voltage capability. Two split resonant capacitors are connected to resonant tank to better achieve soft switching turn-on for active semiconductors. Two different secondary turns were adopted to have low (or high) voltage gain under high (or low) voltage input. Thus, the studied circuit topology could achieve wide zero voltage switching load range and wide voltage input condition. The effectiveness of the presented circuit topology were evaluated and confirmed by the test waveforms with an 800 W prototype with V_{in} = 260 V to 800 V.

Keywords: Resonant converter, wide voltage operation, ZVS, soft switching operation.

1. INTRODUCTION

Over the past few years, high voltage multi-level converters with less voltage rating power devices have been proposed for high power motor drives and power control. Several three-level circuit topologies (Lin and Lu 2000; Malinowski *et al*. 2010; Akagi *et al*. 2011; Lewicki *et al*. 2011) such as series connection of full bridge converters, diode clamp circuit converters and capacitor clamp converters have been developed to lessen the voltage stress on power semiconductors. However, the control scheme of capacitor clamp topologies and series connection of full bridge converters are rather complicated to balance every capacitor voltage. For high frequency operation, the switching losses of power converters are regarded as the serious problem, and so this reduces the circuit efficiency. To better overcome this drawback and improve the converter efficiency, the zero voltage switching techniques have been implemented (Rodrigues *et al*. 2010; Shi and Yang 2013) using the duty cycle control scheme. However, the load range with zero voltage switching operation is limited, and this makes the power switches lose their soft switching operation at the light load condition. Thus, the circuit efficiency of the power converter cannot be improved at the light load condition. Also, the *LLC* converters (Lin and Chen 2015; Haga and Kurokawa 2017; Singh *et al*. 2017) adopt frequency modulation approach to control the input inductive impedance of *LLC* resonant circuit. So, the voltage transfer function of the *LLC* converters can be controlled with variable switching frequency. That is because the resonant converters is operated at the inductive load condition, and the power semiconductors should turn on and off under zero voltage or zero current. To reduce the reliance on the consumption of fossil energy and limit the greenhouse effect, renewable energy conversion with power electronic techniques has been developed. Wind power and solar power conversions are widely used as modern renewables. However, the output voltage of the wind generators and the PV solar cell is not constant. Thus, power electronics with wide input voltage capability have been discussed in several research studies (Wang *et al*. 2017; Lu, Kumar and Afridi 2018; Sun *et al*. 2018; Lin and Lin 2020). The cascaded or series-parallel connection of these several converters were established to achieve wide voltage operation. However, these circuit topologies have the inherent problems of low circuit efficiency or more complicated control algorithms.

In this research study, a new resonant converter designed to achieve wide input voltage and wide soft switching operations was presented and evaluated. Two converter legs were used on the high-voltage side to lessen the voltage rating on power switches. The adopted circuit topology was based on the series resonant converter equipped with two resonant capacitors to reduce the current stress on resonant capacitors. In order to realize wide voltage input between 800 V and 260 V, an auxiliary switch and two different secondary turns of transformer were controlled on the low-voltage side. The high (or low) secondary turns of the transformer was selected and operated under the low (or high) voltage input condition in order to achieve high (or low) converter gain. Optimally speaking, the proposed converter topology had simple circuit structure with reduced component counts. In section II, the circuit topology and the principle of operation are discussed. In section III, the converter analysis and design procedure are provided. Section IV presents the simulated and test results. Finally, the conclusion of the studied converter is drawn and discussed.

2. PRESENTED CIRCUIT TOPOLOGY AND PRINCIPLES OF OPERATION

Fig. 1 gives the circuit structures of the conventional three-level converters with flying capacitor technique, diode clamp technique and series-connected converter. In H-bridge converter, two capacitor voltages must be balanced to have identical voltage stress on each power switch. In flying capacitor three-level converter, the flying capacitor voltage should be controlled at V_{in}/2. In NPC converter, the split input voltages must be controlled at V_{in}/2 in order

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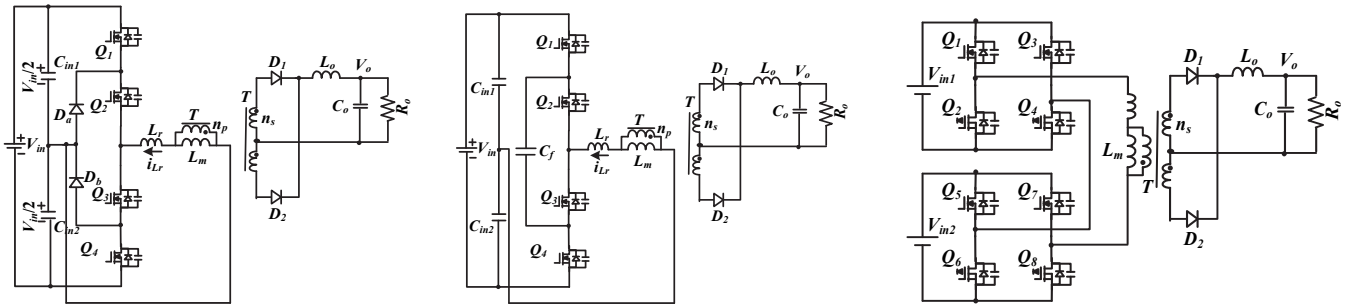
to achieve the balance and symmetry primary side current. Power converters in Fig. 1 are controlled with the pulse-width modulation scheme. The soft switching operation will be lost under low load condition and the input voltage is restricted at 2:1 ($2V_{in,\,min} > V_{in,\,max}$). The presented circuit topology is given in Fig. 2 to realize wide voltage input capability from 260 V to 800 V such as solar cell panel applications. In high-voltage side, the circuit includes two capacitors and two converter legs. Thus, the general 600 V MOSFETs are adopted in the presented circuit. The resonant converter with L_r, L_m, C_{r1}, C_{r2} and $D_1 - D_4$ is controlled to realize soft switching operation on $Q_1 \sim D_1 - D_4$. AC switch S is implemented with two MOSFETs by back-to-back connection in order to select n_s or $2n_s$ winding turns connected to output load with different voltage gains. The presented circuit has two operation ranges: low- and high-voltage input ranges (Fig. 3). Fig. 3(a) gives the proposed converter operated at low-voltage input condition $V_{in,\,L}$ ($V_{in,\,min}$) ~ $2V_{in,\,min}$). Active switch S is conducting and D_3 and D_4 become off. The converter has $2n_s$ secondary turns on the output- the converter voltage gain is $V_o/V_{in,\,L} = G_L(f)n_s/n_p$, where $G_L(f)$ is the voltage transfer function of the converter. Figure 3(b) shows the proposed converter operated at high-voltage input condition $V_{in,\,H}$ ($2V_{in,\,min} \sim 4V_{in,\,min}$). Power switch S and D_1 and D_2 become off. The converter has ns secondary turns on the output-side and the converter voltage gain is $V_o/V_{in,\,H} = G_H(f)n_s/(2n_p)$, where $G_H(f)$ is the voltage transfer function under high-voltage input condition. Since the resonant tank Figs. 3(a) and 3(b) are identical, one can obtain $G_L(f) = G_H(f)$. It can derive that $V_o/V_{in,\,L} = V_o/(V_{in,\,H}/2)$. The frequency control scheme is adopted to drive switches $Q_1 - Q_4$. Switches Q_1 and Q_3 have the same driving signals and Q_2 and Q_4 have the same driving signals.



(a) (b) (c)

Fig. 1 Circuit structures of three-level PWM converters (a) diode clamp (b) flying capacitor (c) series converter.

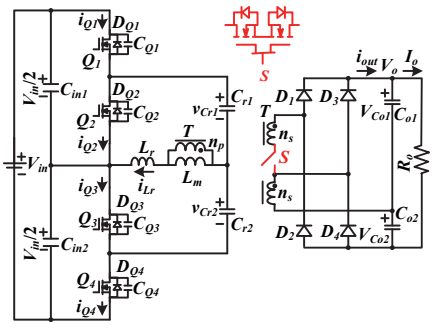
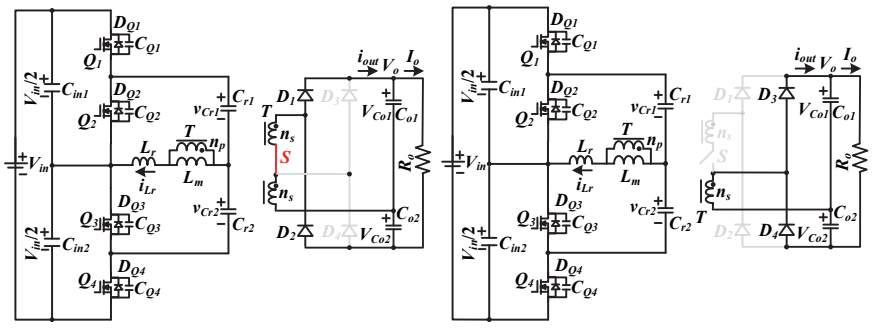


Fig. 2 The circuit configuration of the studied resonant converter



(a) (b)

Fig. 3 Circuit structure and main pulse-width modulation waveforms (a) low-voltage input operation (b) high-voltage input operation

A. Low-Voltage Input Operation (S: on; D_3 & D_4: off; $V_{in,\,L} = V_{in,\,min} \sim 2V_{in,\,min}$)

If V_{in} is greater than $V_{in,\,min}$ and less than $2V_{in,\,min}$, then active device S is turned on. Thus, the rectifier diodes D_3 and D_4 become off (Fig. 3(a)). In the proposed circuit, $C_{oss} = C_{Q1} = \ldots. = C_{Q4}$, $C_{r1} = C_{r2} = C_r$, $C_{in1} = C_{in2}$, $VC_{in1} = VC_{in2} = V_{in}/2$, $C_{o1} = C_{o2}$, and $VC_{o1} = VC_{o2} = V_o/2$. Fig. 4(a) provides the main pulse-width modulation (PWM) waveforms for low-voltage input condition. Fig. 4(b) ~ 4(g) provides the equivalent circuits under f_{sw} (switching frequency) $< f_r$ (resonant frequency).

State 1 [$t_0 \sim t_1$]: In state 1, i_{Lr} discharges C_{Q1} and C_{Q3} to zero voltage at time t_0. Due to D_{Q1} and D_{Q3} are conducting, active switches Q_1 and Q_3 turn on under zero voltage. The drain voltages $v_{Q2,\,ds}$ and $v_{Q4,\,ds}$ equal $V_{in}/2$, and $v_{Cr1} + v_{Cr2} = V_{Cin1} = V_{in}/2$. On the output side, D_1 is conducting so that the transformer secondary voltage equals $V_{Co1} = V_o/2$. The primary side magnetizing voltage v_{Lm} equals $(n_p/2n_s)\,V_o/2$ and the magnetizing current i_{Lm} increases. C_{r1}, C_{r2} and L_r are naturally resonant on the primary side with the resonant frequency $f_{r1} = 1/2\pi\sqrt{L_r(C_{r1}+C_{r2})}$.

State 2 [$t_1 \sim t_2$]: At time t_1, i_{D1} equals zero current and D_1 becomes off with zero current switching. L_r, L_m, C_{r1} and C_{r2} are resonant.

State 3 [$t_2 \sim t_3$]: Q_1 and Q_3 are turned off at time t_2. i_{Lr} discharges C_{Q2} and C_{Q4}. Due to $i_{Lm} > i_{Lr}$, the output diode D_2 is conducting and $v_{Lm} = -(n_p/2n_s)V_o/2$. The magnetizing current i_{Lm} at time t_2 is expressed as.

$$i_{Lm}(t_2) \approx \frac{n_p V_o}{16 n_s L_m f_{sw}} \tag{1}$$

The soft switching turn-on condition of active switches Q_2 and Q_4 are provided in Eq. (2).

$$i_{Lm}(t_2) \geq V_{in}\sqrt{C_{oss}/(L_m + L_r)} \tag{2}$$

where $C_{Q1} = \ldots = C_{Q4} = C_{oss}$. The maximum magnetizing inductance L_m is given in Eq. (3).

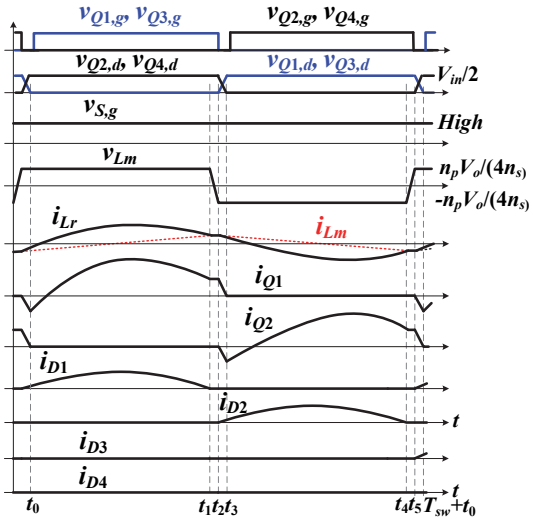
$$L_m \leq \frac{n_p V_o t_d}{16 V_{in} f_s n_s C_{oss}} \tag{3}$$

where t_d is the dead time between Q_2 and Q_1.

State 4 [$t_3 \sim t_4$]: The voltages $vC_{Q2}(t_3) = vC_{Q4}(t_3) = 0$ so that D_{Q2} and D_{Q4} will conduct due to $i_{Lr}(t_3) > 0$. The drain-to-source voltages $v_{Q2,ds}$ and $vQ_{4,ds}$ keep at zero voltage Q_2 and Q_4 can achieve soft switching turn-on after time t_3. During the state 4, $v_{Q1,ds} = v_{Q3,ds} = V_{in}/2$ and $v_{Cr1} + v_{Cr2} = VC_{in2} = V_{in}/2$. Owing to $i_{Lm} > i_{Lr}$, D_2 conducts and $v_{Lm} = -(n_p/2n_s)V_o/2$. Components L_r, C_{r1} and C_{r2} are resonant.

State 5 [$t_4 \sim t_5$]: The diode current $i_{D2}(t_4) = 0$ and D_2 becomes off with zero current switching. In state 4, L_r, L_m, C_{r1} and C_{r2} are resonant.

State 6 [$t_5 \sim T_{sw} + t_0$]: At time t_5, Q_2 and Q_4 turn off. $i_{Lr}(t_5) < 0$ and C_{Q1} and C_{Q3} are discharged. Due to $i_{Lr} > i_{Lm}$ after time t_5, D_1 is conducting and $v_{Lm} = (n_p/2n_s)V_o/2$.



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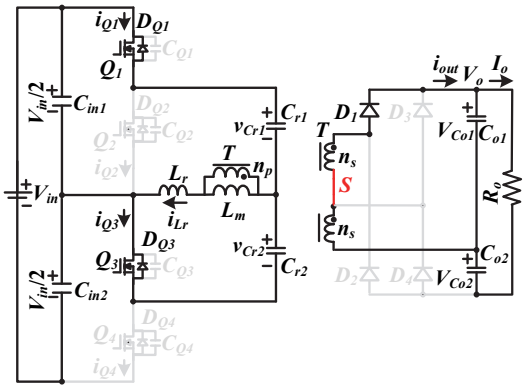

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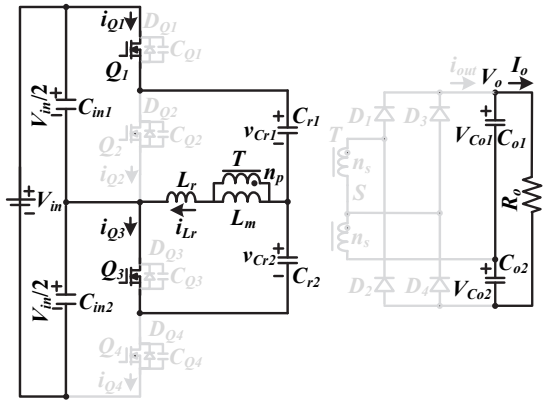

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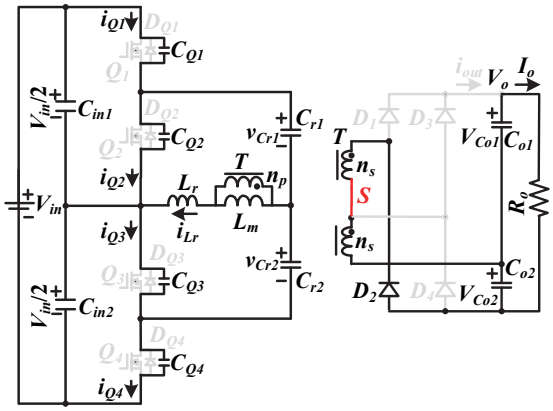

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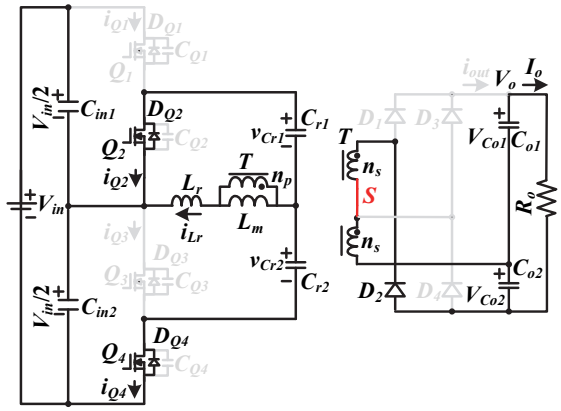

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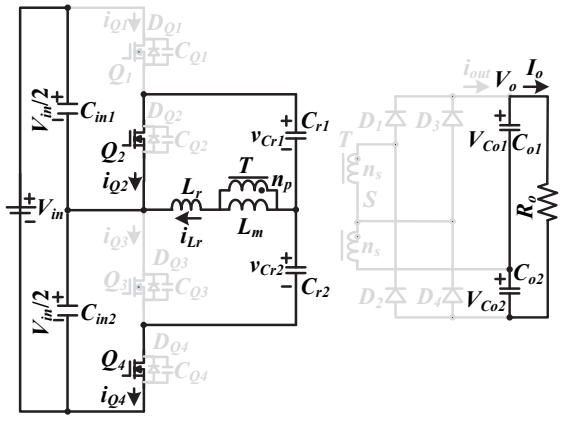

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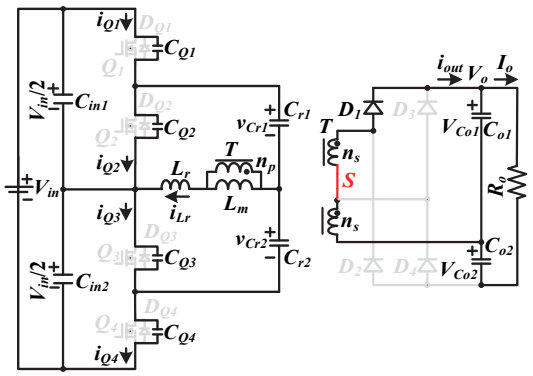

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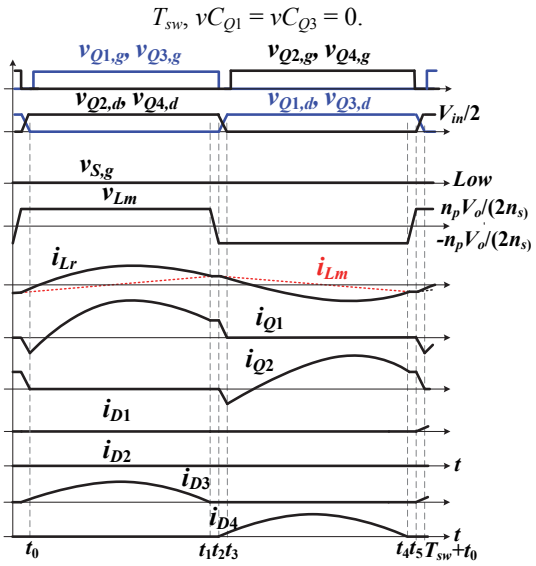

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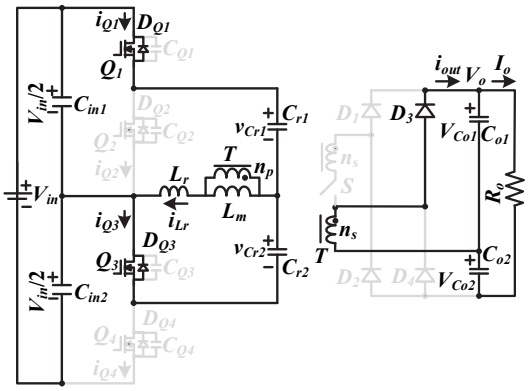

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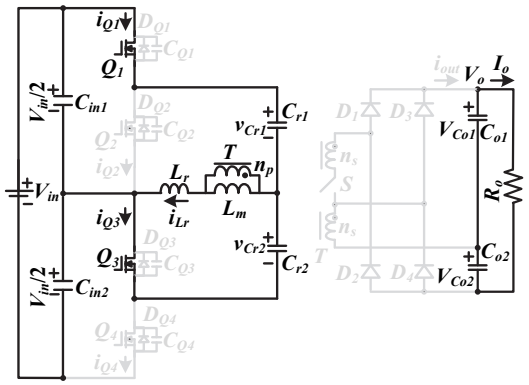

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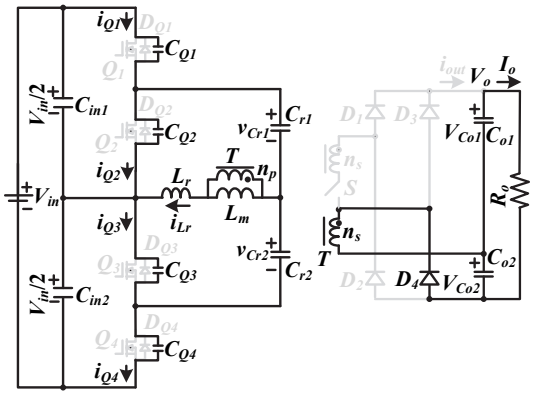


Fig. 4 Converter under low-voltage input operation (a) pulse-width modulation signals (b) circuit for state-1 (c) circuit for state-2 (d) circuit for state-3 (e) circuit for state-4 (f) circuit for state-5 (g) circuit for state-6.

B. High-Voltage Input Operation (S: off; D_1 & D_2: off; $V_{in,H} = 2V_{in,min} \sim 4V_{in,min}$)

If the input voltage V_{in} is less than $4V_{in,min}$ and $4V_{in,min}$ greater than $2V_{in,min}$, S is turned off. Thus, the rectifier diodes D_1 and D_2 become off (Fig. 3(b)). From Fig. 3(b), it is clear that the turns-ratio on the equivalent circuit is np/ns for high input voltage operation. The PWM signals and circuit for each state under high-voltage input condition are provided in Fig. 5.

State 1 [$t_0 \sim t_1$]: The voltages $vC_{Q1}(t_0) = vC_{Q3}(t_0) = 0$. Since $i_{Lr}(t_0) < 0$ and D_{Q1} and D_{Q3} are conducting, Q_1 and Q_3 are turned on under zero voltage. The drain voltages $v_{Q2,ds} = v_{Q4,ds} = vC_{r1} + vC_{r2} = V_{in}/2$. The magnetizing voltage $v_{Lm} = (n_p/n_s)V_o/2$ and i_{Lm} increases.

State 2 [$t_1 \sim t_2$]: The diode current $i_{D3}(t_1)$ is zero and D_3 becomes off. Components C_{r1}, C_{r2}, L_r and L_m are resonant.

State 3 [$t_2 \sim t_3$]: Q_1 and Q_3 turn off at time t_2. C_{Q2} and C_{Q4} (C_{Q1} and C_{Q3}) discharge (charge) in this state. Since $i_{Lm} > i_{Lr}$, diode D_4 becomes forward biased and $v_{Lm} = -(n_p/n_s)V_o/2$. The magnetizing current $i_{Lm}(t_2)$ is calculated as.

$$i_{Lm}(t_2) \approx \frac{n_p V_o}{8 n_s L_m f_{sw}} \quad (4)$$

The maximum magnetizing inductance L_m for high-voltage input operation is expressed in Eq. (5).

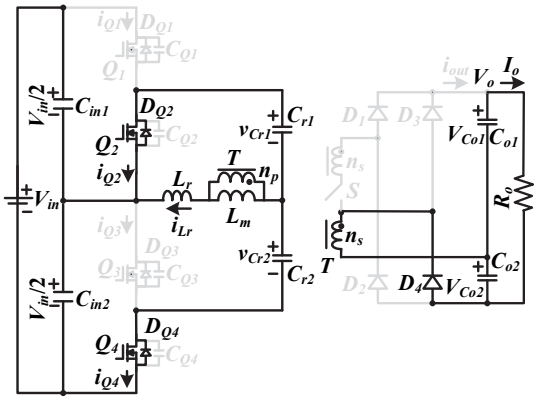
$$i_{Lm}(t_2) \approx \frac{n_p V_o}{8 n_s L_m f_{sw}} \quad (5)$$

State 4 [$t_3 \sim t_4$]: The voltages $vC_{Q2}(t_3) = vC_{Q4}(t_3) = 0$ so that D_{Q2} and D_{Q4} become forward biased due to $i_{Lr}(t_3)$ is positive. Thus, Q_2 and Q_3 achieve soft switching turn-on after time t_3. Since $i_{Lm} > i_{Lr}$, D_4 is forward biased and $v_{Lm} = -(n_p/n_s)V_o/2$.

State 5 [$t_4 \sim t_5$]: The current $i_{D4}(t_4) = 0$ and D_4 becomes reverse biased. C_{r1}, C_{r2}, L_r and L_m are resonant.

State 6 [$t_5 \sim T_{sw} + t_0$]: At time t_5, Q_2 and Q_4 are turned off. Due to $i_{Lr}(t_5) < 0$, i_{Lr} discharges C_{Q1} and C_{Q3}. Since $i_{Lr} > i_{Lm}$ after time t_5, D_3 becomes forward biased and $v_{Lm} = (n_p/n_s)V_o/2$. At time $t_0 +$

(d)



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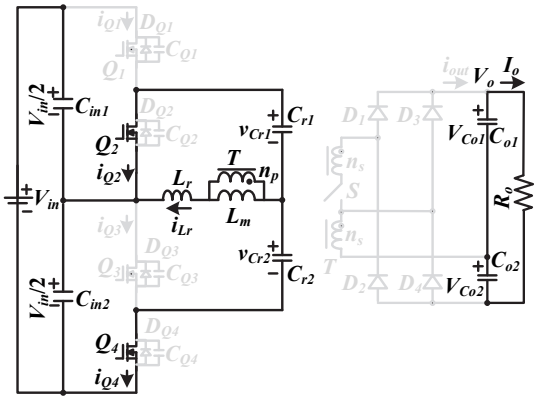

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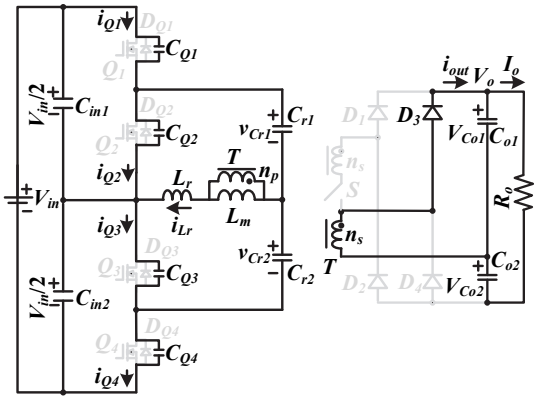

(g)

Fig. 5 Converter under high-voltage input operation (a) pulse-width modulation signals (b) circuit for state-1 (c) circuit for state-2 (d) circuit for state-3 (e) circuit for state-4 (f) circuit for state-5 (g) circuit for state-6.

3. CONVERTER ANALYSIS AND DESIGN PROCEDURE

The analysis of the circuit characteristic of the studied circuit heavily depends on the FHA (fundamental harmonic analysis). On the output-side, the switch S is off or on to achieve different voltage gains under the high-voltage input and the low-voltage input conditions. Based on the FHA's approach, the relationship between the primary-side resistance R_{ac} and the output resistance R_o is expressed in Eq. (6).

$$R_{ac}=\begin{cases}\dfrac{(n_p/n_s)^2 R_o}{2\pi^2}, & S\ on\\ \dfrac{2\,(n_p/n_s)^2 R_o}{\pi^2}, & S\ off\end{cases} \tag{6}$$

Thus, the equivalent resonant circuit of the studied converter is consisted of L_r, $C_{r1}+C_{r2}$, R_{ac} and K_m. The voltage gain with frequency modulation is expressed in Eq. (7)

$$|G|=\frac{1}{\sqrt{\left[1+\frac{1}{l_n}\frac{f_n^2-1}{f_n^2}\right]^2+a^2\left(\frac{f_n^2-1}{f_n}\right)^2}}=\begin{cases}\dfrac{n_p V_o}{n_s V_{in}}, & S\,on\\ \dfrac{2n_p V_o}{n_s V_{in}}, & S\ off\end{cases} \tag{7}$$

where $l_n = L_m/L_r$, $f_n = f_{sw}/f_r$ and $a=\sqrt{L_r/2C_r}/R_{ac}$. From Eq. (7), V_o can be obtained in Eq. (8).

$$V_o=\begin{cases}\dfrac{n_s V_{in}}{n_p\sqrt{\left[1+\frac{1}{l_n}\frac{f_n^2-1}{f_n^2}\right]^2+a^2\left(\frac{f_n^2-1}{f_n}\right)^2}}, & S\ on\\ \dfrac{n_s V_{in}}{2n_p\sqrt{\left[1+\frac{1}{l_n}\frac{f_n^2-1}{f_n^2}\right]^2+a^2\left(\frac{f_n^2-1}{f_n}\right)^2}}, & S\ off\end{cases} \tag{8}$$

The design steps of the presented converter are provided and discussed. The input and output specifications are: V_{in} = 260 V ~ 800 V, V_o = 48 V, P_o = 800 W and f_{r1} = 100 *k*Hz. The adopted inductance ratio $l_n = L_m/L_r = 5$. If 260 V < V_{in} < 420 V (low-voltage input condition), S is turned on. If 420 V < V_{in} < 800 V (high-voltage input condition), then S is turned off. The voltage gain at V_{in} = 800 V condition is designed to be unity. Thus, the transformer turns-ratio n_p/n_s can be obtained in Eq. (9).

$$n_p/n_s = V_{in,max}/2V_o \approx 8.33 \tag{9}$$

The prototype transformer has primary turns n_p = 24 and secondary turns n_s = 3. From Eq. (6), R_{ac} for at the maximum output power is obtained in Eq. (10).

$$R_{ac} = 2(n_p/n_s)^2 R_o/\pi^2 \approx 37.35\,\Omega \tag{10}$$

In this prototype, the selected quality factor a = 0.2 and l_n = 5. Thus, the components L_r, L_m, C_{r1} and C_{r2} are calculated in Eqs. (11) ~ (13).

$$L_r = aR_{ac}/(2\pi f_{r1}) \approx 12\mu \tag{11}$$

$$L_m = l_n L_r = 60\mu H \tag{12}$$

$$C_{r1} = C_{r2} = 1/(8\pi^2 L_r f_{r1}^2) \approx 105nF \tag{13}$$

The complete elements of the test circuit are given in Table 1.

Table 1 Components of the Test Circuit

Symbol	Parameter
V_{in}	260 V ~ 800 V
V_o	48 V
I_o	16.67 A
f_{r1}	100 kHz
C_{o1}, C_{o2}	540 µF / 100 V
C_{in1}, C_{in2}	180 µF/450 V
C_{r1}, C_{r2}	105 nF
$Q_1 \sim Q_4$	STF40N60M2 (650 V/ 22 A)
S	IXTP160N075T (75 V/ 160 A)
L_r	12 µH
L_m	60 µH
$D_1 \sim D_4$	S60SC6M (60 V/60 A)
$n_p : n_s : n_s$	24 : 3 : 3

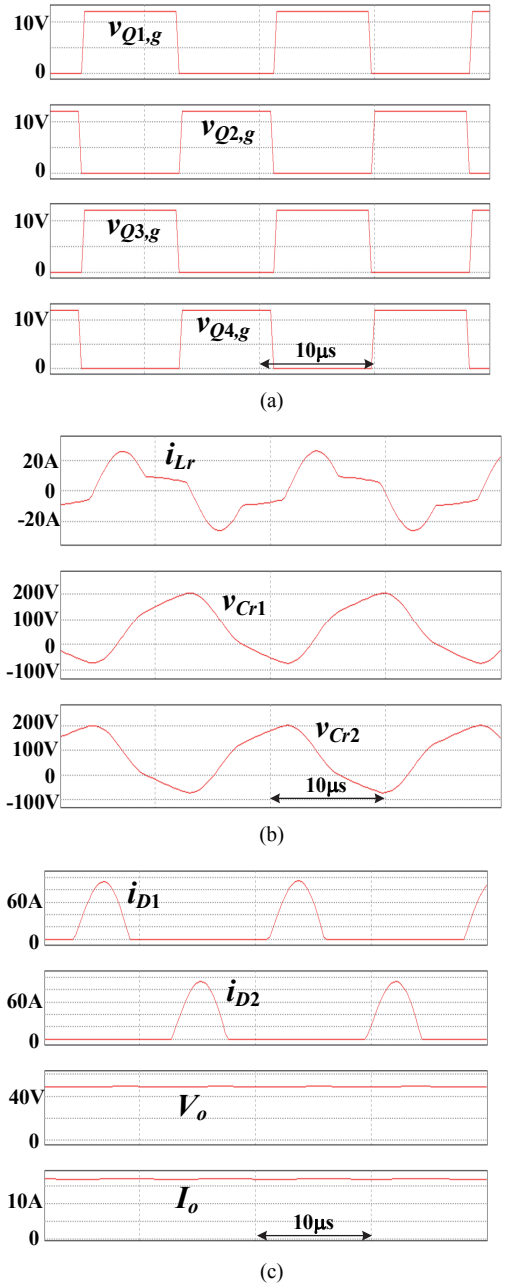

Fig. 6 Simulated waveforms at V_{in} = 260 V and the full load (a) $Q_1 - Q_4$ (b) i_{Lr}, vC_{r1} and vC_{r2} (c) i_{D1}, i_{D2}, V_o and I_o.

4. SIMULATED AND TEST RESULTS

The simulated and experimental waveforms are provided and discussed to demonstrate the performance of the studied circuit topology. First, the simulation results are given in Figs. 6 and 8 for low-voltage and high-voltage input conditions. Figure 6 provides the simulated waveforms under the minimum input voltage case V_{in} = 260 V (low-voltage input case). The gating signals of four power switches are given in Fig. 6(a). The primary side waveforms of the isolated transformer are provided in Fig. 6(b). Under low-voltage input operation, D_3 and D_4 become and only D_1 and D_2 are conducting. Fig. 6(c) illustrates the simulated waveforms of i_{D1}, i_{D2}, V_o and I_o. It is clear that D_1 and D_2 achieve soft switching turn-off. Figure 7 gives the test results at V_{in} = 260 V and the full load. Compared the simulated and experimental results in Figs. 6 and 7, the test results and the theoretical waveforms are agreed each other. Figs. 8 and 9 provide the simulated and test waveforms at V_{in} = 800 V (maximum input voltage). Since the resonant converter operated at V_{in} = 800 V input has less voltage gain, the switching frequency at V_{in} = 800 V condition (Fig. 9(a)) is higher than the frequency (Fig. 7(a)) at V_{in} = 260 V case. It is also obvious the diodes D_3 and D_4 turned off with hard switching (Fig. 9(c)) due to f_{sw} (switching frequency) > f_{r1} (resonant frequency). From the simulated and test results shown in Figs. 6 ~ 9, the studied converter can achieve wide-voltage input operation.

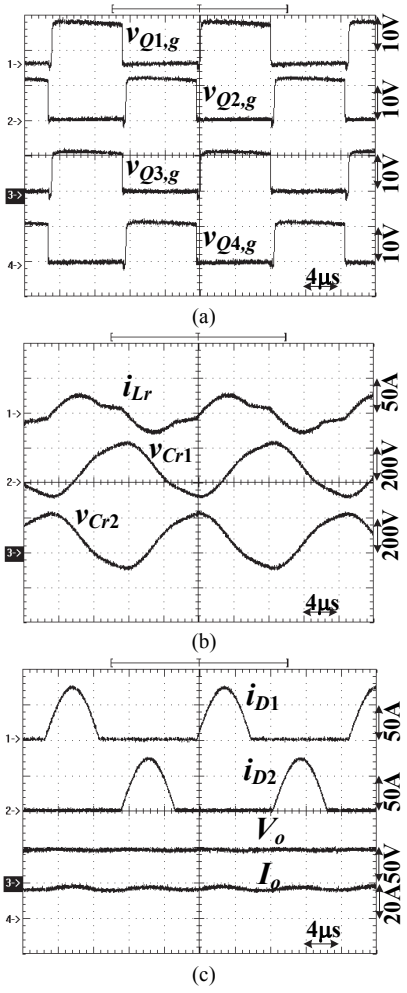

Fig. 7 Experimental results at *Vin* = 260 V and the full load (a) $Q_1 - Q_4$ (b) i_{Lr}, v_{Cr1} and v_{Cr2} (c) i_{D1}, i_{D2}, V_o and I_o.

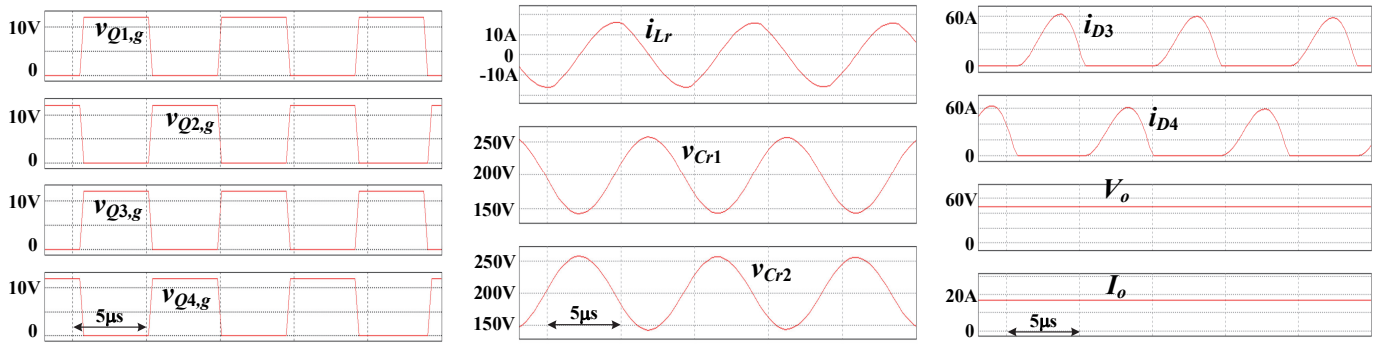

Fig. 8 Simulated waveforms at V_{in} = 800 V and the full load (a) $Q_1 - Q_4$ (b) i_{Lr}, vC_{r1} and vC_{r2} (c) i_{D3}, i_{D4}, V_o and I_o.

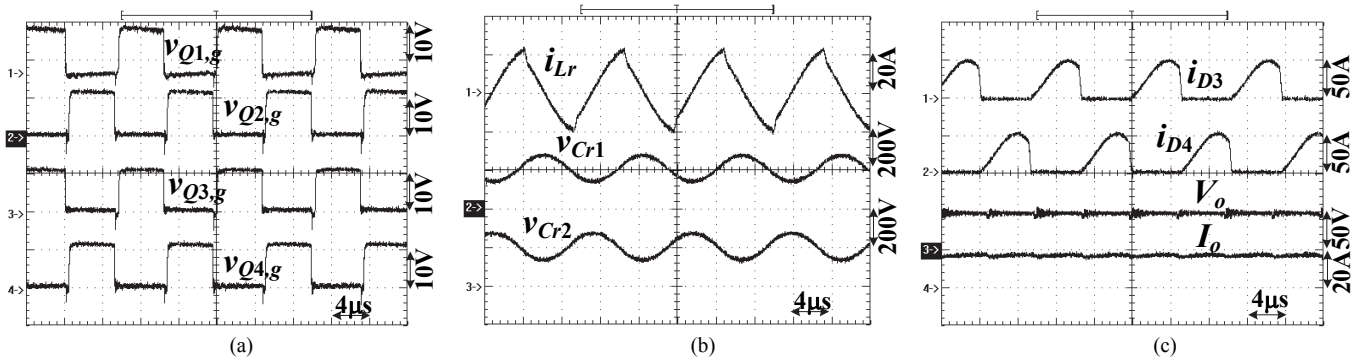

Fig. 9 Experimental results at V_{in} = 800 V and the full load (a) $Q_1 - Q_4$ (b) i_{Lr}, vC_{r1} and vC_{r2} (c) i_{D3}, i_{D4}, V_o and I_o.

5. CONCLUSION

A hybrid LLC resonant converter with different transformer winding turns is discussed and presented to achieve wide-voltage input operation. Two series-connected converter legs are adopted to decrease the voltage rating on active semiconductors. Two resonant capacitors are adopted in the resonant tank to operate as the resonant components and to balance two input capacitors. One auxiliary switch is used on low-voltage side to change the turn-ratio of transformer. Therefore, the drawback of conventional resonant converter is improved. To investigated the performance of the presented circuit, the simulated and test waveforms are provided. The experimental waveforms agree the simulated waveforms and the theoretical analysis.

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