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High Step-Up Converter with Leakage Inductance Energy Recycling

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ABSTRACT

This paper proposes and tests a novel high step-up converter. Using a coupling inductor and energy-transfer capacitors, the tested prototype realized high step-up voltage gains, and recycled leakage inductance energy. A TMS320F28335 digital signal processor was used as a control kernel. The operating principles of the proposed circuit were described and analyzed, then the effectiveness of the working prototype was discussed.

Keywords: High step-up converter, Leakage inductance energy recycling.

1. INTRODUCTION

Traditional high-step up boost converters are limited to a gain multiplier of approximately four-times. This is due to the presence of parasitic components (Erickson and Maksimovic 2001). In recent years, various high step-up converters have been proposed and applied in renewable energy conversion systems. For non-isolated circuits, such as KY converters and their derivatives (Hwu and Yau 2009, Hwu and Yau 2010, Hwu *et al*. 2011, Hwu and Tu 2012, Hwu and Peng 2014, Hwu and Jiang 2014, Hwu *et al*. 2013, Hwu and Yau 2014), an energy-transfer capacitor circuit in combination with a boost inductor or coupled inductor can collectively achieve a higher voltage gain. The literature for such designs (Hwu and Yau 2014) shows a circuit topology using coupled inductors, which employs an active voltage clamp to suppress voltage spikes across the main switch. However, the high step-up converters exhibited by (Hwu and Peng 2014, Pan and Lai, 2010, Ajami *et al*. 2015, Zhou *et al*. 2014, Kim and Moon 2015, Evran and Aydemir 2014, all have quite cumbersome operating states. There are a large number of components, but the circuit analysis becomes complex. Hence, they are not well suited to industrial use. Other studies (Chen and Xu 2014) show circuit topologies using inductors and coupled inductors. These apply methods of leakage inductance energy recovery, but again, the excessive number of components detrimentally affects overall conversion efficiency. Another study by (Chen *et al*. 2015) utilized coupled inductors and energy-transfer capacitors to achieve a higher voltage gain. The number of components in this case was lower, but it was not able to recover leakage inductance energy.

A different approach by (Liang *et al*. 2014) used a circuit topology with more than three switches. The converter had low efficiency compared to the single-switch variant, and has no discernable advantages in industrial settings, furthermore, the unit cost for these is relatively high. (Hagar and Lehn 2014; Hou and Chen 2014) wrote papers showing that the superposition of multiple sets of energy-transfer capacitors can produce a high voltage gain. (Hagar and Lehn 2014) configured capacitors in series and parallel to produce voltage boosting and bucking effects. In (Hou and Chen 2014), however, the capacitor-diode modules were overlapped to produce a high voltage gain. Research by (Tseng *et al*. 2015) also demonstrated a high voltage gain by superimposing more than two energy-transfer capacitors. This type of converter requires an output capacitor in parallel at the output, to reduce the output voltage ripple. (Tang *et al*. 2014; Tang *et al*. 2015) showed a circuit composed of several capacitors and diodes that could also achieve voltage boosting; this type of circuit they referred to as a voltage doubler circuit as the combination of inductors and diodes produced a voltage doubling effect. The approach used in (Tang *et al*. 2015) was a modification of (Tang *et al*. 2014). The initial design used many components, but the revised version was more flexible and used fewer components.

Given the existing research on high step-up converters, such as the one found in (Hwu and Yau 2010), this paper makes adaptations using one coupled inductor, and two energy-transfer capacitors to achieve a high voltage gain, while also recycling leakage inductance energy.

2. ANALYSIS OF THE PROPOSED HIGH STEP-UP CONVERTER

2.1 Proposed Circuit

Fig. 1 shows the proposed high step-up converter, which has a zero current cut-off at the diode, continuous input current, and leakage inductance energy recovery. This circuit is composed of one coupled inductor (N_1 and N_2), two energy-transfer capacitors C_1 and C_2, one switch S_1, three diodes D_1, D_2 and D_3, and one output capacitor C_o. The input voltage is represented by V_i, the output voltage is indicated by V_o, and the output load resistor is defined as R_o.

Prior to analyzing the operational principles of the circuit, a brief explanation of the related symbol definitions and assumptions is offered:

(1) The capacitance of the energy-transfer capacitors C_1 and C_2 are large enough to make the output voltage acquire a certain value.

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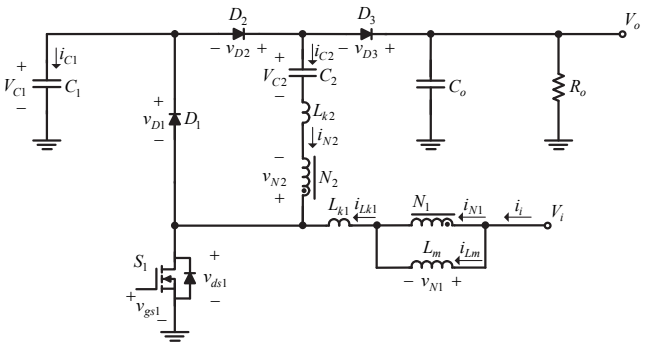

Fig. 1 Proposed high step-up converter.

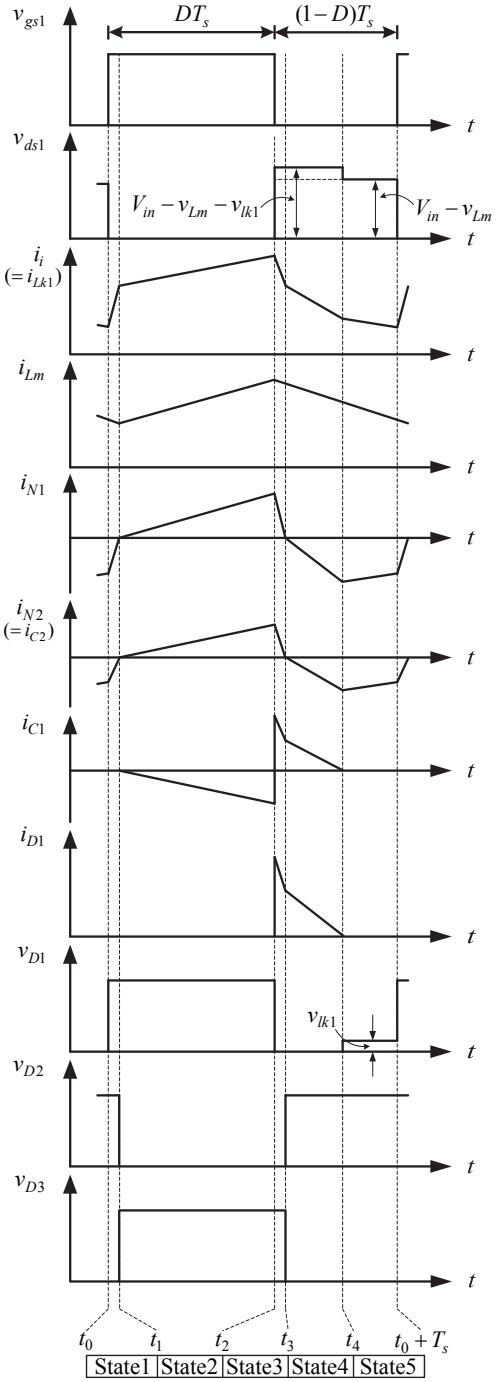

Fig. 2 Circuit waveform stages for the proposed prototype.

(2) N_1 and N_2 are the number of turns on the primary and secondary sides of the coupled inductor, respectively, and the turns ratio is given by N_2/N_1.
(3) v_{gs1} is the driving signal of the switch S_1, v_{ds1} is the voltage across the switch S_1, v_{Lm} is the voltage across the magnetizing inductor L_m, v_{N1} is the voltage across the primary winding N_1, v_{N2} is the voltage across the secondary winding N_2, v_{D1} is the voltage across the diode D_1, v_{D2} is the voltage across the diode D_2, and v_{D3} is the voltage across the diode D_3.
(4) i_i is the input current, i_{Lm} is the current flowing through the magnetizing inductor L_m, i_{N1} is the current flowing through the primary side, i_{N2} is the current flowing through the secondary side, i_{C1} is the current in the energy-transfer capacitor C_1, and i_{C2} is the current in the energy-transfer capacitor C_2.
(5) T_s is the switching period, DT_s is the turn-on time, and $(1–D)$ T_s is the turn-off time.
(6) All diodes and switches are assumed to be ideal components.
(7) The circuit is assumed to operate in continuous current mode (CCM).
(8) The operating principle of the converter is analyzed in a steady state. Fig. 2 shows the simulated waveforms relevant to the design.

2.2 Operating Principle

State 1 [$t_0 \le t \le t_1$]: As shown in Fig. 3, switch S_1 is turned on, diode D_3 is turned on, and the diodes D_1 and D_2 are turned off. At this time, leakage inductor L_{k2} is demagnetized. The voltage across N_2 (v_{N2}) is negative, making the voltage across N_1, where the magnetizing inductor Lm (v_{N1}) is, also negative. This demagnetizes L_m. At the same time, the voltage across the leakage inductor L_{k1} is given by the sum of the input voltage V_i and the voltage v_{N1}, so the leakage inductor L_{k1} becomes magnetized. At this time, the energy required by the load is provided by the energy-transfer capacitor C_2, L_m, and L_{k2}. By t_1, the demagnetization of L_{k2} is complete, that is, the current in L_{k2} reaches zero, and state 1 ends.

State 2 [$t_1 \le t \le t_2$]: As shown in Fig. 4, switch S_1 is turned on, diode D_2 is turned on, and diodes D_1 and D_3 are turned off. At this time, the voltage across the magnetizing inductor Lm and leakage inductance L_{k1} feed the input voltage V_i, so that the magnetizing inductor L_m and the leakage inductance L_{k1} become magnetized. At the same time, the energy-transfer capacitor C_1 releases energy to the leakage inductance L_{k2} and the energy-transfer capacitor C_2, via the secondary side of N_2, so that the voltage across the leakage inductor L_{k2} is positive. This magnetizes L_{k2}. At this time, the energy load required is provided by the output capacitor C_o. At t_2, switch S_1 is turned off, ending state 2.

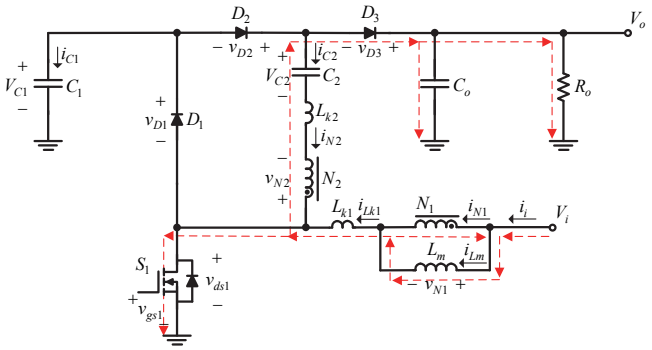

Fig. 3 Current flow during state 1.

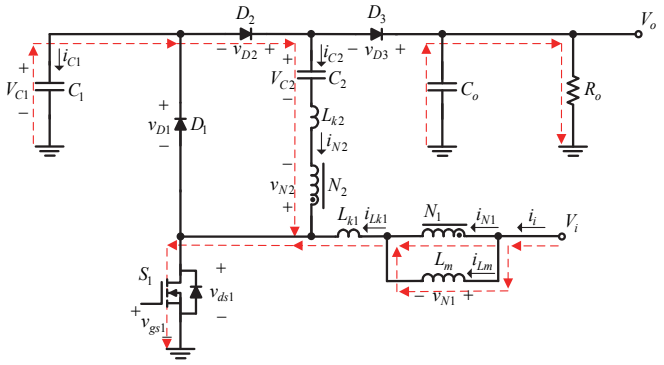

Fig. 4 Current flow during state 2.

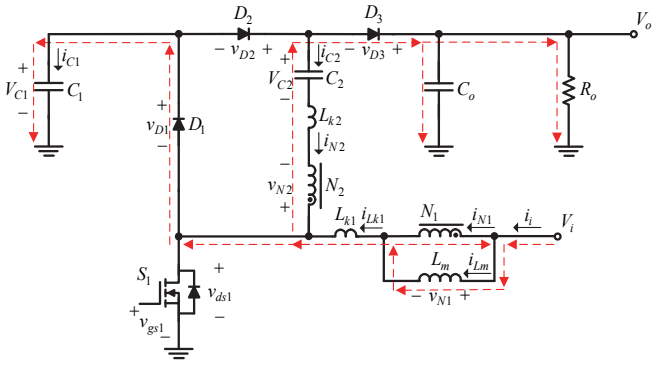

Fig. 6 Current flow during state 4.

State 3 [$t_2 \le t \le t_3$]: As shown in Fig. 5, switch S_1 is turned off, diodes D_1 and D_2 are turned on, and diode D_3 is turned off. Since D_1 is turned on, the voltage across the leakage inductor L_{k2} is negative. This causes the leakage inductance L_{k2} to demagnetize in a positive direction. At this time, L_{k2} releases energy to the energy-transfer capacitor C_2 via the secondary side of N_2. Since the voltage across the magnetizing inductor Lm and leakage inductance L_{k1} are negative, that is, the input voltage V_i minus the voltage across C_1, (V_{C1}), the magnetizing inductance L_m and the leakage inductance L_{k1} are demagnetized. At this time, the energy required by the load is provided by the output capacitor C_o. At time t_3, the demagnetization of the leakage inductance L_{k2} is complete, such that the current in the leakage inductor L_{k2} is zero, and state 3 ends.

State 4 [$t_3 \le t \le t_4$]: As shown in Fig. 6, switch S1 is turned off, diodes D_1 and D_3 are turned on, and diode D_2 is turned off. At this time, the voltage across the magnetizing inductor Lm and leakage inductor L_{k1} are determined by the input voltage V_i, minus the voltage across the energy-transfer capacitor C_1 (V_{C1}). This means L_m and L_{k1} are demagnetized, and C_1 becomes charged. At the same time, the voltage across the leakage inductor L_{k2} is V_o + v_{N2}-V_{C1}-V_{C2} where $v_{N2} < 0$. Where the voltage across the leakage inductor L_{k2} is negative, L_{k2} becomes magnetized in the opposite direction. The energy required by the load is provided by the input voltage V_i, the energy-transfer capacitor C_2 and the magnetizing inductor L_m through the primary side N_1, and the secondary side N_2. At time t_4, the current i_{C1} is zero, the diode D_1 is cut off, and state 4 ends.

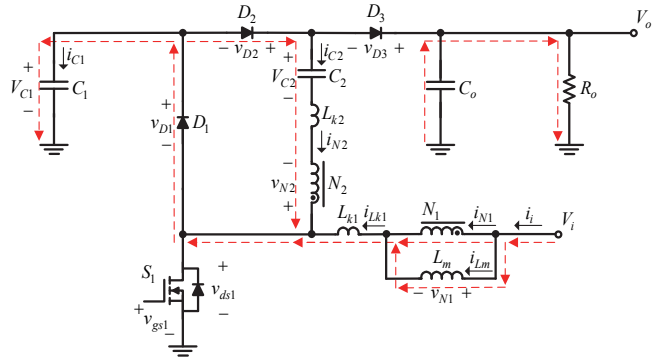

Fig. 5 Current flow in state 3.

State 5 [$t_4 \le t \le t_5 + T_s$]: As shown in Fig. 7, switch S_1 is turned off, diode D_3 is turned on, and diodes D_1 and D_2 are turned off. At this time, the voltage across the magnetizing inductor L_m is still negative, so L_m is demagnetized. At the same time, the energy load required is determined by the input voltage V_i, the energy-transfer capacitor C_2 the magnetizing inductor L_m, the leakage inductor L_{k1} and the leakage inductor L_{k2} via the primary side N_1 and the secondary side N_2. Once switch S_1 is turned on at time $t_5 + T_s$, state 5 ends, the circuit operation returns to state 1, and the next cycle commences.

2.3 Derivation of Voltage Gain

In order to simplify analysis of the voltage gain, the leakage inductances L_{k1} and L_{k2} are negligible, this means that in states 1 and 3 they can be omitted. From Fig. 4, which shows state 2, the following equations can be obtained:

$$\begin{cases} v_{N1} = V_i \\ V_{C2} = V_{C1} + v_{N2} \end{cases} \tag{1}$$

From Figs. 6 and 7, the equations pertaining to states 4 and 5 are

$$\begin{cases} v_{N1} = V_i - V_{C1} \\ v_{N1} = V_i + V_{C2} - v_{N2} - V_o \end{cases} \tag{2}$$

Where

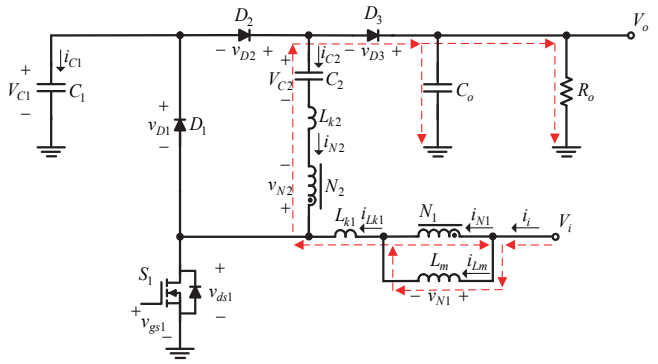

Fig. 7 Current flow during state 5.

$$\begin{cases} v_{N2} = v_{N1} \times n \\ V_{C1} = V_{C2} - v_{N2} \end{cases} \tag{3}$$

Substituting (3) into (2) produces

$$\begin{cases} v_{N1} = V_i - V_{C1} \\ v_{N1} = V_i + V_{C1}(1+n) - V_o \end{cases} \tag{4}$$

The voltage across the magnetizing inductor L_m must obey the steady state voltage-second balance:

$$V_i D + (V_i - V_{C1})\ (1-D) = 0 \tag{5}$$

$$V_i D + \left[V_i + V_{C1}(1+n) - V_o\right]\ (1-D) = 0 \tag{6}$$

Rearranging (5) yields

$$V_{C1} = \frac{V_i}{1-D} \tag{7}$$

Substituting (7) into (6) yields a voltage gain defined by

$$\frac{V_o}{V_i} = \frac{2+n}{1-D} \tag{8}$$

2.4 Boundary conditions for a coupled inductor current

For calculation purposes it is assumed that there is no power conversion loss, making input power equal to output power. Following (8), the input current can thus be expressed by

$$I_i = \frac{2+n}{1-D} I_o \tag{9}$$

where

$$I_o = \frac{V_o}{R_o} \tag{10}$$

Therefore, based on (10), (9) can be expressed as

$$I_i = \frac{2+n}{1-D} \times \frac{V_o}{R_o} \tag{11}$$

In addition, the average value of i_{Lm}, called I_{Lm}, can be represented by

$$I_{Lm} = I_i - I_{N1} \tag{12}$$

I_{N1} is the average value of i_{N1}, where n (= N_2/N_1). The average value of i_{N2} is referred to as I_{N2}, which is the same as the average value of i_{C2}, referred to as I_{C2}.

$$I_{N1} = \frac{N_2}{N_1} \times I_{N2} = \frac{N_2}{N_1} \times I_{C2} \tag{13}$$

According to ampere-second balance, the average current I_{C2} is zero, and (12) can be rewritten as

$$I_{Lm} = I_i \tag{14}$$

Substituting (11) into (14) yields

$$I_{Lm} = \frac{2+n}{1-D} \times \frac{V_o}{R_o} \tag{15}$$

The current ripple in the magnetizing inductor Δi_{Lm} can be obtained by

$$\Delta i_{Lm} = \frac{v_{Lm} \Delta t}{L_m} = \frac{V_i D T_s}{L_m} \tag{16}$$

Therefore as $2I_{L_m} \geq \Delta i_{Lm}$, the magnetizing inductor L_m works in continuous conduction mode (CCM), and the corresponding inequality can be obtained:

$$\begin{aligned} & 2I_{L_m} \geq \Delta i_{Lm} \\ \Rightarrow\ & 2 \times \frac{2+n}{1-D} \times \frac{V_o}{R_o} \geq \frac{V_i D T_s}{L_m} \\ \Rightarrow\ & \frac{2L_m}{R_o T_s} \geq \frac{(1-D)DV_i}{(2+n)V_o} \\ \Rightarrow\ & \frac{2L_m}{R_o T_s} \geq \frac{(1-D)D}{2+n} \times \frac{1-D}{2+n} \\ \Rightarrow\ & \frac{2L_m}{R_o T_s} \geq \frac{(1-D)^2 D}{(2+n)^2} \\ \Rightarrow\ & K \geq K_{crit}(D) \end{aligned} \tag{17}$$

where $K = \dfrac{2L_m}{R_o T_s}$ and .

According to (17) and where n = 2, and $K \geq K_{crit}(D)$, the converter continues in continuous conduction mode (CCM); otherwise, it switches to discontinuous conduction mode (DCM). Therefore, the boundary curve for operating modes can be plotted as shown in Fig. 8.

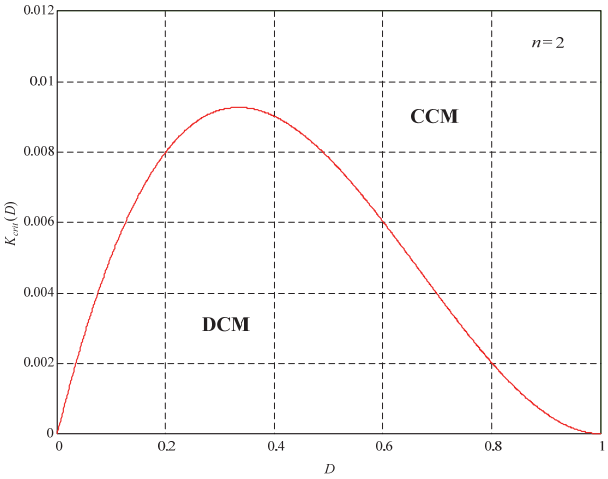

Fig. 8 Boundary curve for operating modes

2.5 Comparisons of the proposed topology and existing designs

Comparisons between the proposed circuit and existing designs follow. Factors compared include voltage gain, number of components used, voltage stress on switches and diodes, and leakage inductance recycling. All data is shown in full in Table 1. The curve of voltage gain versus duty cycle is shown in Fig. 9.

Fig. 9 displays the relationship between voltage gain (V_o/V_i) and duty cycle (D) for the circuits presented in Table 1. The converters all operate in CCM and the turns ratio is 2. Fig. 9, shows that as the value of D falls below 0.675, the voltage gain of the proposed circuit becomes smaller than that of the circuit shown in [9]. However, where the value of D is greater than 0.675, the voltage gain of the proposed circuit is better than other designs.

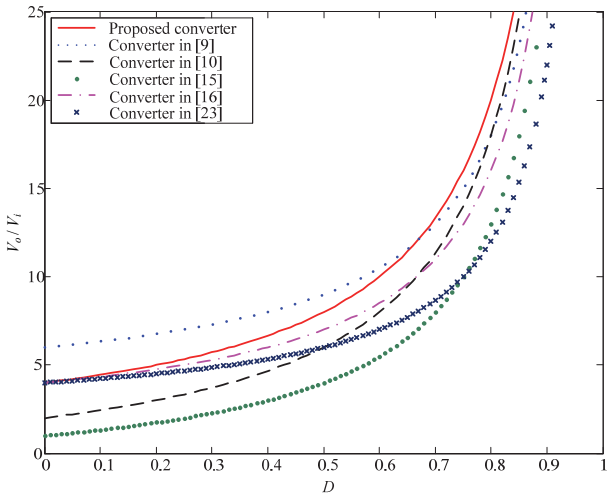

Fig. 9 Voltage gain V_o/V_i comparison of the proposed circuit and existing designs using data drawn from Table 1.

Table 1 Comparison of the proposed circuit with existing designs.

Literature	Voltage gain	No.	Switch voltage stress	Diode voltage stress	Leakage inductance energy recycling
[9]	$\frac{2-D}{1-D}(1+n)$	10	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	$V_{D1}=V_i\left(\frac{n+2-D}{1-D}-1\right)$, $V_{D2}=\frac{nV_i}{1-D}$, $V_{Do}=V_o-V_i(1+n)$	Yes
[10]	$\frac{2+nD}{1-D}$	14	$V_{ds1}=V_{ds2}=\frac{V_o}{2}-\frac{nDV_i}{2(1-D)}$	$V_{D1}=V_o-\frac{nDV_i}{1-D}$, $V_{D2}=\frac{V_o}{2}-\frac{nDV_i}{2(1-D)}$	No
[15]	$\frac{1+nD}{1-D}$	8	$V_{ds1}=\frac{V_i}{1-D}$	$V_{D1}=V_o+nV_i-\frac{V_i}{1-D}$, $V_{Dc}=\frac{V_i}{1-D}$	No
[16]	$\frac{2+n-D}{1-D}$	6	$V_{ds1}=\frac{V_i}{1-D}$	$V_{D1}=V_o-V_i$, $V_{D2}=V_o-V_i$	No
[23]	$\frac{2}{1-D}+n$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	$V_{D1}=V_o-nV_i+\frac{nV_i-V_i}{1-D}$, $V_{D1}=V_o-V_i\left(\frac{1}{1-D}+n\right)$	No
Proposed	$\frac{2+n}{1-D}$	8	$V_{ds1}=\frac{V_i}{1-D}$	$V_{D1}=\frac{V_i}{1-D}$, $V_{D2}=\frac{1+n}{1-D}V_i$, $V_{D3}=V_o-\frac{V_i}{1-D}$	Yes

3. DESIGN CONSIDERATIONS

3.1 System and Component Specifications

Tables 2 and 3 show the system and component specifications, respectively, for the proposed circuit.

Table 2 System specifications

Operating mode	CCM
Input voltage (V_i)	56V
Rated output voltage (V_o)	380V
Rated output current ($I_{o,\,rated}$) / Rated output power ($P_{o,\,rated}$)	526.32mA/200W
Min. output current ($I_{o,min}$) / Min. output power ($P_{o,min}$)	52.632mA/20W
Switching frequency(f_s)/Period (T_s)	100kHz/10μs

Table 3 Component specifications

Components		Specifications
MOSFET switch S_1		IRFB4227PBF
Diodes	D_1	SBR30200CT
	D_2, D_3	STPSC606D
Capacitors	C_1	68μF electrolytic capacitor
	C_2	33μF electrolytic capacitor
Output capacitor C_o		120μF electrolytic capacitor
Coupled inductor		Core：PC44PQ35/35Z-12, n = 1.5, L_m = 456μH, L_{lk1} = 1.094μH, L_{lk1} = 2.575μH, k = 0.9976
Gate driver		TC4420
DSP		TMS320F28335

3.2 Determination of Duty Cycle and Coupled Inductor Turns Ratio

From (8), the duty cycle D can be obtained by

$$D=\frac{V_o-V_i\,(2+n)}{V_o} \tag{18}$$

Sequentially, it is assumed that the value of D is between 0.4 and 0.5, and by substituting the system specifications into (18), the following formulation can be obtained

$$\begin{aligned} &0.4\le\frac{V_o-V_i\,(2+n)}{V_o}\le 0.5\\ &\Rightarrow 0.4\le\frac{380-56\,(2+n)}{380}\le 0.5\\ &\Rightarrow 1.393\le n\le 2.071 \end{aligned} \tag{19}$$

Given a turns ratio of 1.5, this can be substituted into (8), and the value of D can be calculated as 0.484 (20):

$$D=\frac{V_o-V_i\,(2+n)}{V_o}=\frac{380-56\,(2+1.5)}{380}=0.484 \tag{20}$$

3.3 Determination of Coupled Inductor Magnetizing inductance

According to (16), if the coupled inductor operates in a positive current, the value of the magnetizing inductance L_m should satisfy the following inequality:

$$\begin{aligned} &L_m\ge\frac{(1-D)^2D}{(2+n)^2}\times\frac{R_{o,max}T_s}{2}\\ &\Rightarrow L_m\ge\frac{(1-D)^2D}{(2+n)^2}\times\frac{V_o}{I_{o,min}}\times\frac{T_s}{2} \end{aligned} \tag{21}$$

where R_o, max is the load resistance under light load, and I_o, min is the load current under light load.

Substituting the system parameters from Table 2 and (20) into (21) yields

$$\begin{aligned} &L_m\ge\frac{(1-0.484)^2\times 0.484}{(2+1.5)^2}\times\frac{380}{52.632m}\times\frac{10\mu}{2}\\ &\Rightarrow L_m\ge 379.621\mu H \end{aligned} \tag{22}$$

Thus, the value of Lm is 454.91.

3.4 Determination of Voltage Stresses on Switches and Diodes

Via the operating principle analyses for states 3, 4 and 5, the voltage stresses on S_1, D_1, D_2 and D_3 can be determined by:

$$\begin{aligned} V_{ds1}&=\frac{V_i}{1-D}\\ &=\frac{56}{1-0.484}\cong 108.5V \end{aligned} \tag{23}$$

$$V_{D1}=V_{C1}=\frac{V_i}{1-D}=\frac{56}{1-0.484}=108.5V \tag{24}$$

$$V_{D2}=\frac{1+n}{1-D}V_i=\frac{1+1.5}{1-0.484}\times 56=271.32V \tag{25}$$

$$\begin{aligned} V_{D3}&=V_o-\frac{1}{1-D}V_i\\ &=380-\frac{1}{1-0.484}\times 56=271.47V \end{aligned} \tag{26}$$

In practice, there will be many parasitic components which may cause excessive voltage spikes, potentially causing damage to the switches, increasing the conduction loss. This means the rated voltages of the switches should be between 1.5 ~ 2.5 times the calculated (expected) maximum voltage stress, and in addition, they should ideally have a lower on-resistance. For switch S_1, an IRFB4227PBF manufactured by International Rectifier Co., was chosen.

For selection of the diode D_1, it is again necessary to consider the possibility of excessive voltage spikes that may cause the diode to malfunction. Excessive conduction loss may easily cause the diode to overheat. To account for this, a Schottky Diode with a low forward conduction voltage *VF* is preferable. The rated voltage of the diode should also be approximately 1.5 ~ 2.5 times over the calculated maximum voltage stress, with a lower *VF* where possible. For diode D_1, a SBR30200CT manufactured by STMicroelectronics Co., was chosen.

4. EXPERIMENTAL RESULTS

4.1 Steady-State Waveforms

Figs. 10, 18 and 26 show that there is no voltage spike across v_{ds1} at switch S_1. The main reason is that when switch S_1 changes state, it excites the energy-transfer capacitor C_1. The current ids1 is the sum of the current i_{lk1} (= *ii*) and the current i_{N2}. The currents i_{Lk1} and i_{N2} increase as the output load current increases. Under light loads, the current i_{ds1} is different than when the system is running at 50% to 100% load.

Figs. 11, 19 and 27 show that there is no voltage spike at diode D_1. The main reason for this is that when the switch S_1 is turned off, the magnetizing inductance L_m and the leakage inductor L_{k1} are demagnetized. They charge the energy-transfer capacitor C_1 through diode D_1, so that when switch S_1 turns off, the charging current receives a current spike that increases as the load increases. As the current in C_1 drops to zero, diode D_1 which has zero current switching (ZCS), turns-off across the entire load range.

Figs. 12, 20 and 28 show that the voltage across diode D_2 does not experience a voltage spike. When switch S_1 is turned on, the current i_{D2} flows through diode D_2 in the opposite direction. The energy-transfer capacitor C_2 begins to charge and produces a current spike, that current spike increases as the load increases.

Figs. 13, 21 and 29 show that the voltage across diode D_3 does not spike. Under light loads, current i_{D3} is different than when the system is running at 50% to 100% load.

Figs. 14, 22 and 30 show that the voltage at the energy-transfer capacitor C_1 assumes a given value for different load levels. When the main power switch S_1 is turned on, the current flowing into C_1 exhibits a negative current spike, and the energy stored in the leakage inductor L_{k2} and the energy stored in C_1 charges the energy-transfer capacitor C_2. This produces the leakage inductance recovery system. When the main power switch S_1 is turned off, the current in C_1 experiences a positive current spike due to the demagnetization of L_{k1}.

Figs. 15, 23 and 31 show that the voltage across C_2 assumes a given value for different load levels. When the main power switch S_1 is turned on, the current flowing through C_2 has a positive current spike as shown in Fig. 12. When S_1 is turned off, current i_{C2}, current i_{N2} and i_{D3} are the same and the output is equal to the load, as shown in Fig. 13.

Figs. 16, 24 and 32 show that the input current ii and the current i_{N2} both increase with the increase in output current. Under light loads, the currents ii and i_{N2} are different than when the system is running at 50% to 100% load.

Figs. 17, 25 and 33 show that the output voltage V_o and the output current I_o are approximately stable for certain values, even using different loads.

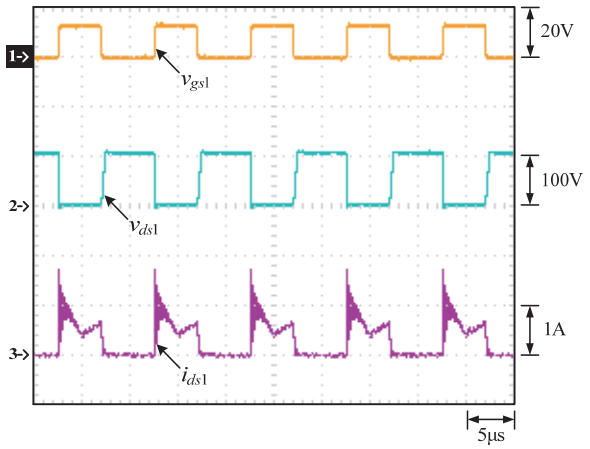

Fig. 10 Waveforms under 10% load: (1) v_{gs1}; (2) v_{ds1}; (3) i_{ds1}.

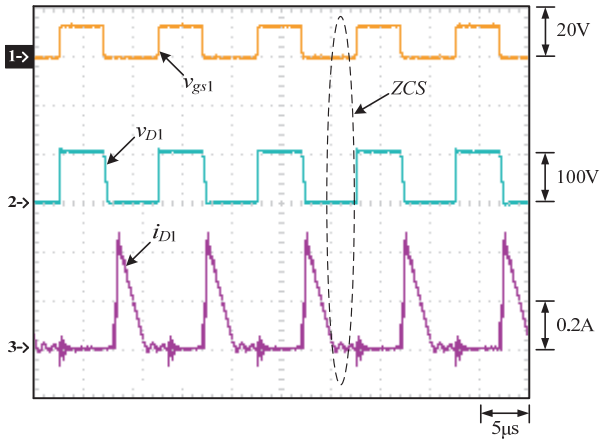

Fig. 11 Waveforms under 10% load: (1) v_{gs1}; (2) v_{D1}; (3) i_{D1}.

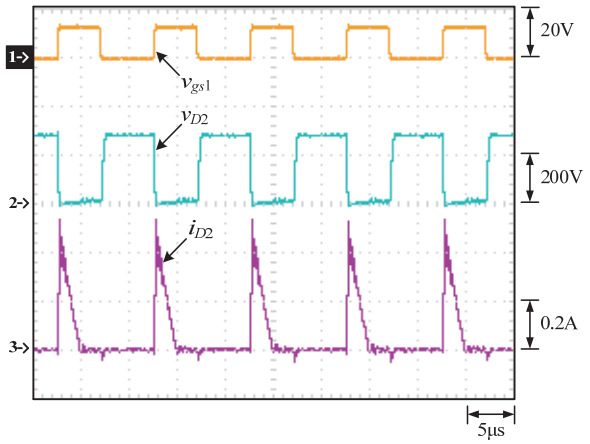

Fig. 12 Waveforms at 10% load: (1) v_{gs1}; (2) v_{D2}; (3) i_{D2}.

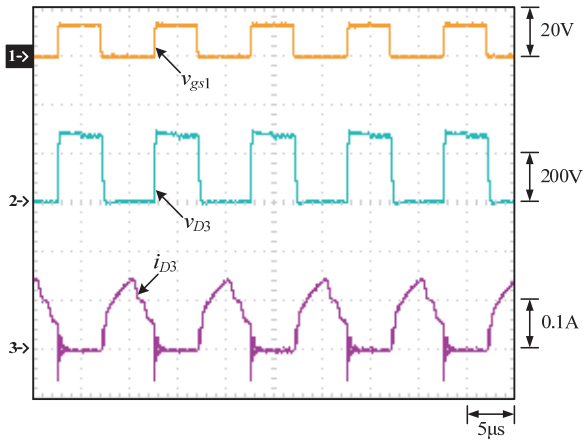

Fig. 13 Waveforms at 10% load: (1) v_{gs1}; (2) v_{D3}; (3) i_{D3}.

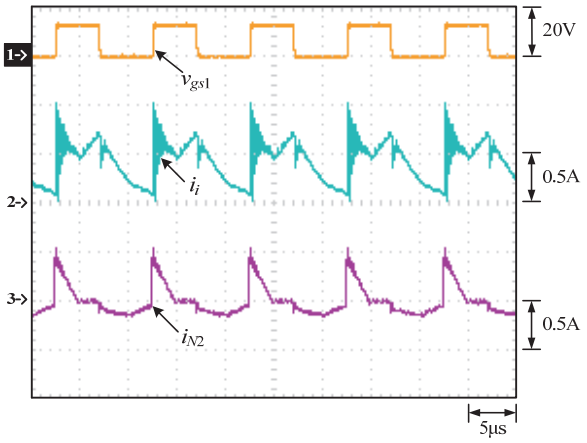

Fig. 16 Waveforms at 10% load: (1) v_{gs1}; (2) i_i; (3) i_{N2}.

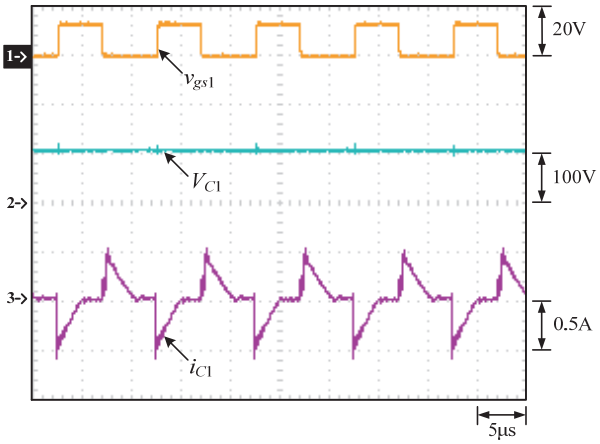

Fig. 14 Waveforms at 10% load: (1) v_{gs1}; (2) V_{C1}; (3) i_{C1}.

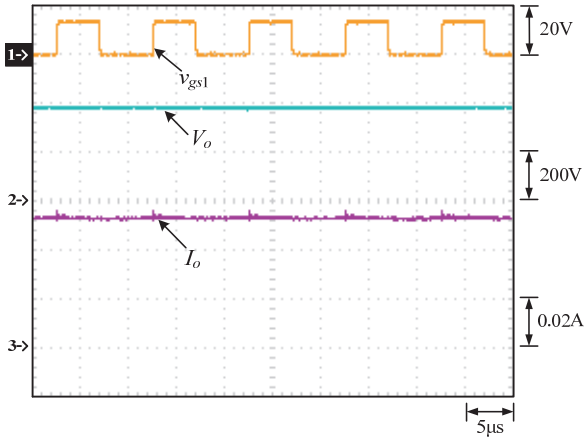

Fig.17 Waveforms at 10% load: (1) v_{gs1}; (2) V_o; (3) I_o.

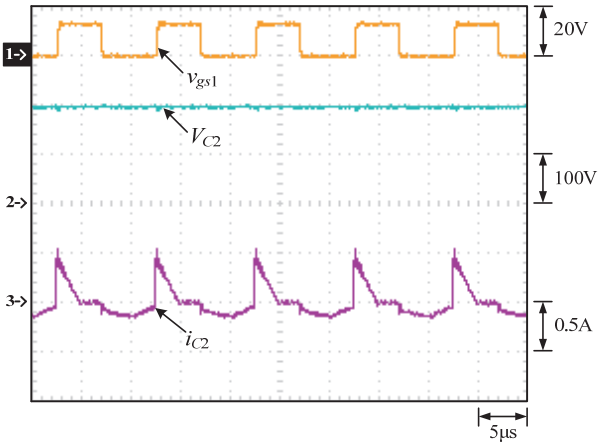

Fig. 15 Waveforms at 10% load: (1) v_{gs1}; (2) V_{C2}; (3) i_{C2}.

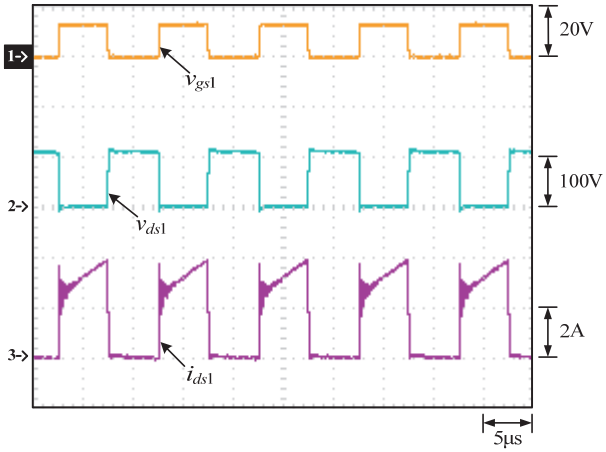

Fig. 18 Waveforms at 50% load: (1) v_{gs1}; (2) v_{ds1}; (3) i_{ds1}.

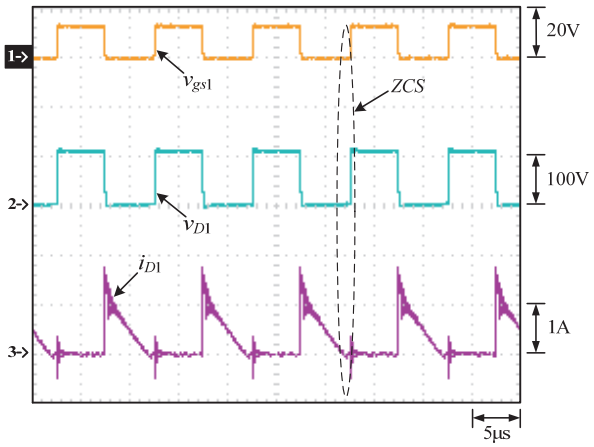

Fig. 19 Waveforms at 50% load: (1) v_{gs1}; (2) v_{D1}; (3) i_{D1}.

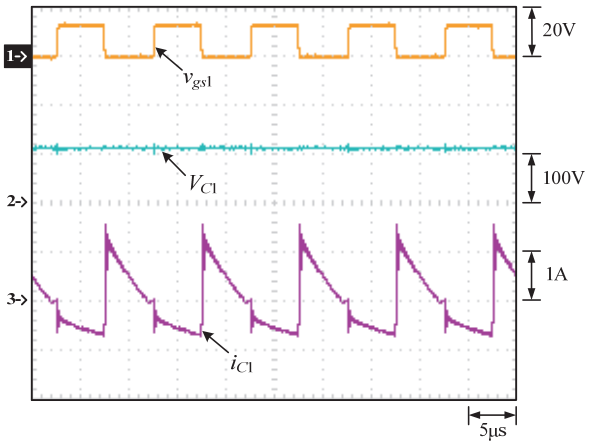

Fig. 22 Waveforms at 50% load: (1) v_{gs1}; (2) V_{C1}; (3) i_{C1}.

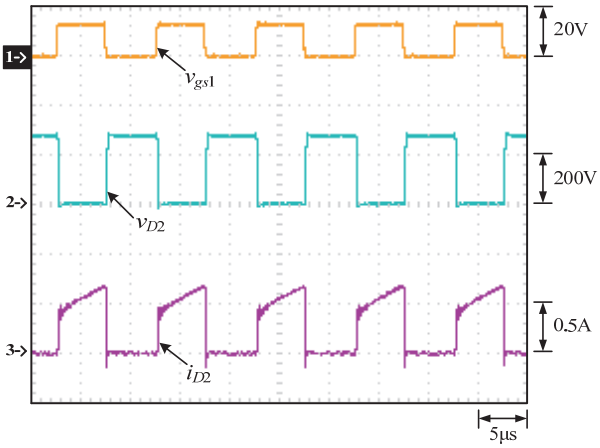

Fig. 20 Waveforms at 50% load: (1) v_{gs1}; (2) v_{D2}; (3) i_{D2}.

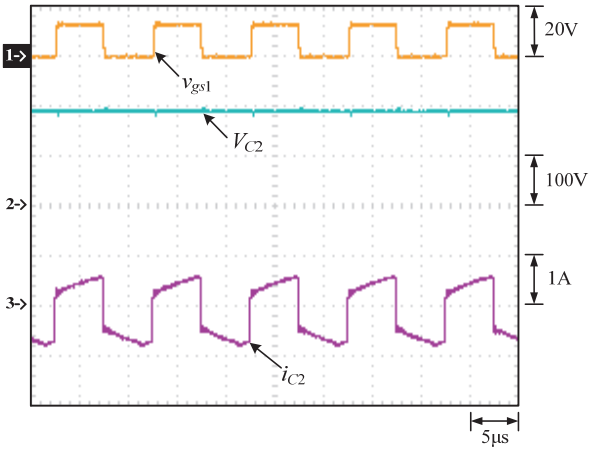

Fig. 23 Waveforms at 50% load: (1) v_{gs1}; (2) V_{C2}; (3) i_{C2}.

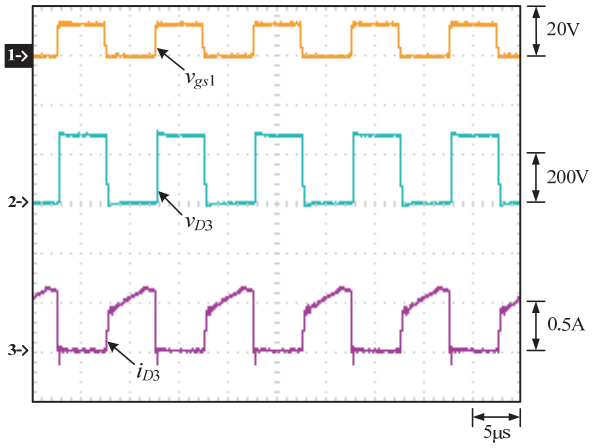

Fig. 21 Waveforms at 50% load: (1) v_{gs1}; (2) v_{D3}; (3) i_{D3}.

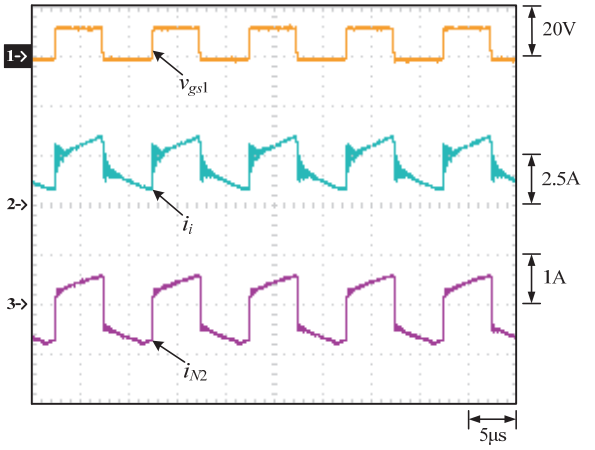

Fig. 24 Waveforms at 50% load: (1) v_{gs1}; (2) i_i; (3) i_{N2}.

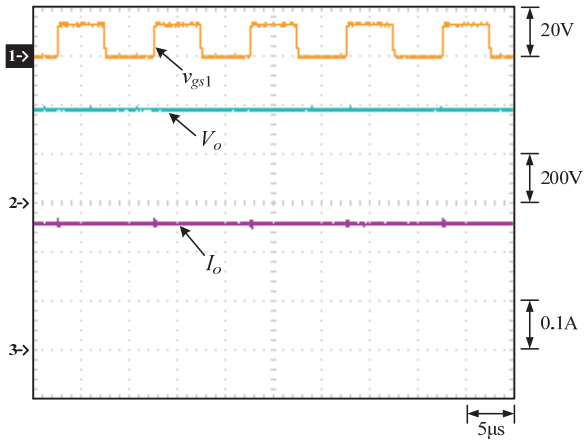

Fig. 25 Waveforms at 50% load: (1) v_{gs1}; (2) V_o; (3) I_o.

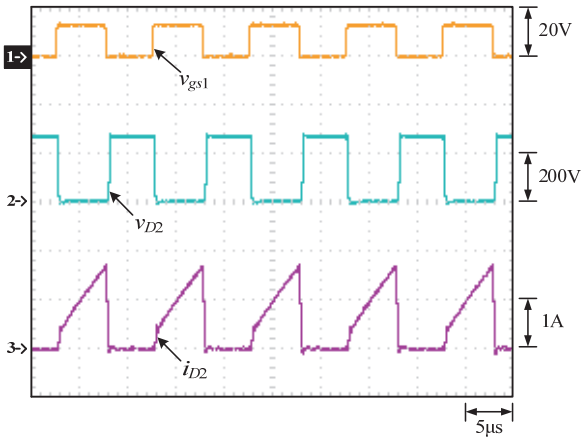

Fig. 28 Waveforms at % load: (1) v_{gs1}; (2) v_{D2}; (3) i_{D2}.

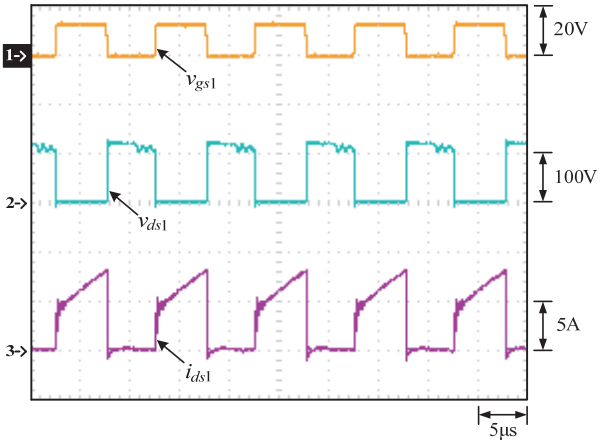

Fig. 26 Waveforms at 100% load: (1) v_{gs1}; (2) v_{ds1}; (3) i_{ds1}.

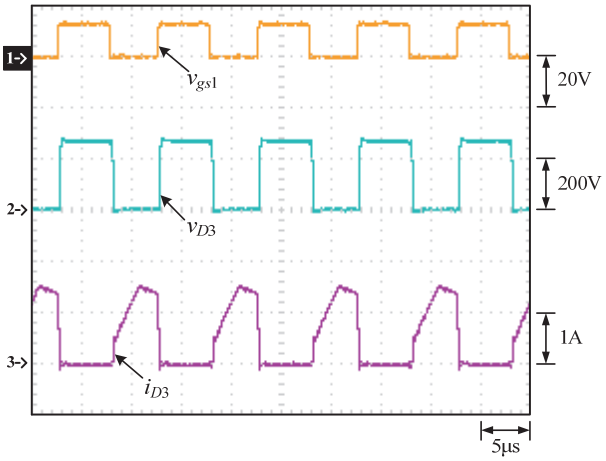

Fig. 29 Waveforms at 100% load: (1) v_{gs1}; (2) v_{D3}; (3) i_{D3}.

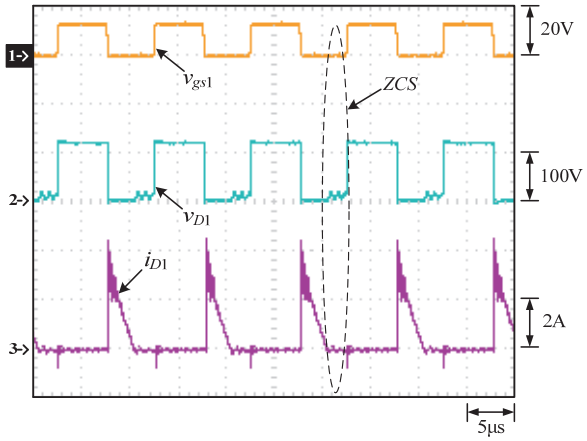

Fig. 27 Waveforms at 100% load: (1) v_{gs1}; (2) v_{D1}; (3) i_{D1}.

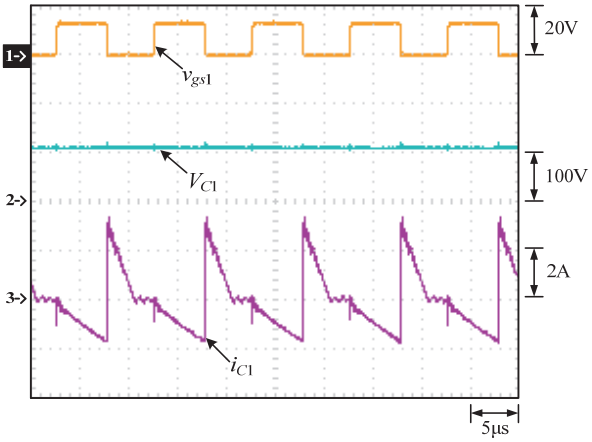

Fig. 30 Waveforms at 100% load: (1) v_{gs1}; (2) V_{C1}; (3) i_{C1}.

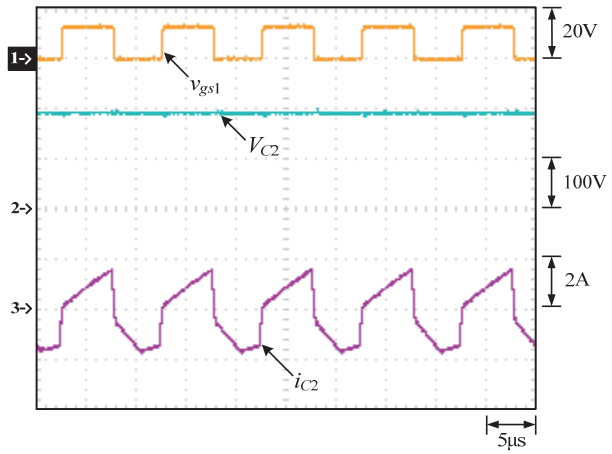

Fig. 31 Waveforms at 100% load: (1) v_{gs1}; (2) V_{C2}; (3) i_{C2}.

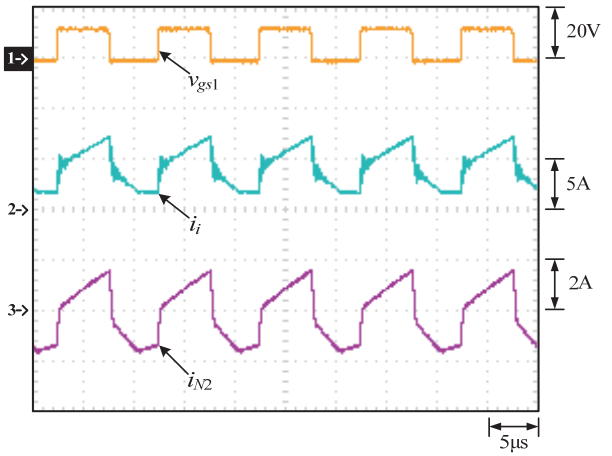

Fig. 32 Waveforms at 100% load: (1) v_{gs1}; (2) i_i; (3) i_{N2}.

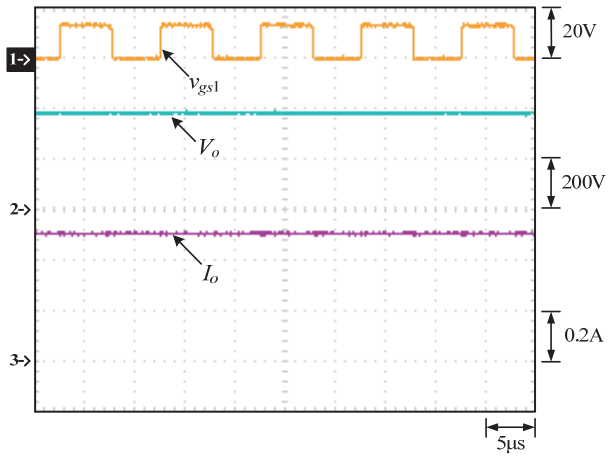

Fig. 33 Waveforms at 100% load: (1) v_{gs1}; (2) V_o; (3) I_o.

4.2 Transient Load Response

Fig. 34 displays the transient load response at 10% to 50% of rated load. From this figure, it can be seen that the output voltage recovery time is about 100ms, and that there is a change in output voltage of about −1.6%. Fig. 35 displays the transient load response at 50% to 10% of rated load. From this figure, it can be seen that the output voltage recovery time is about 110ms, and the gain in output voltage is about 1.3 %.

Fig. 36 displays the transient load response at 50% to 100% of rated load. From this figure, it can be seen that the output voltage recovery time is about 30ms, and the change in output voltage is approximately −0.53%. Fig. 37 displays the transient load at 100% to 50% of rated load. From this figure, it can be seen that the output voltage recovery time is about 40ms, and the gain in output voltage is about 0.66%.

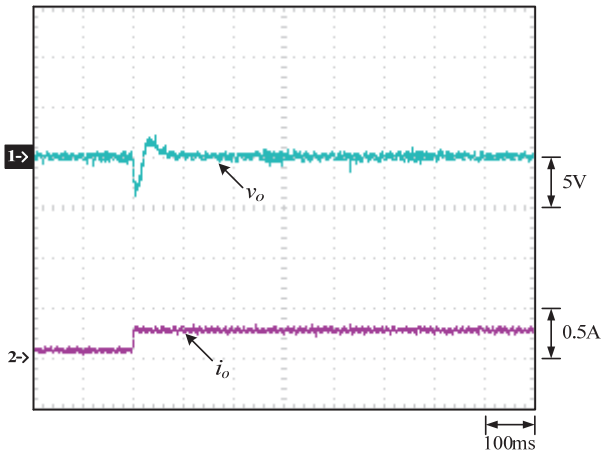

Fig. 34 Transient load response at 10% to 50% load.

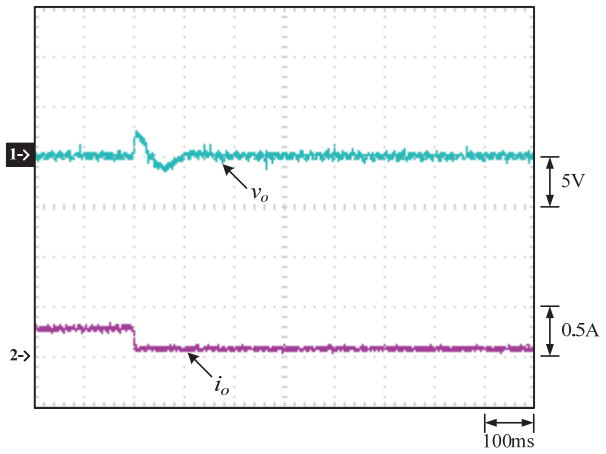

Fig. 35 Transient load response at 50% to 10% load.

Fig. 38 displays the transient load response at 10% to 100% of rated load. From this figure, it can be seen that the output voltage recovery time is about 100ms, and change in output voltage is approximately −1.85%. Fig. 39 displays the transient load at 100% to 50% of rated load. From this figure, it can be seen that the output voltage recovery time is about 110ms, and the gain in output voltage is about 1.6%.

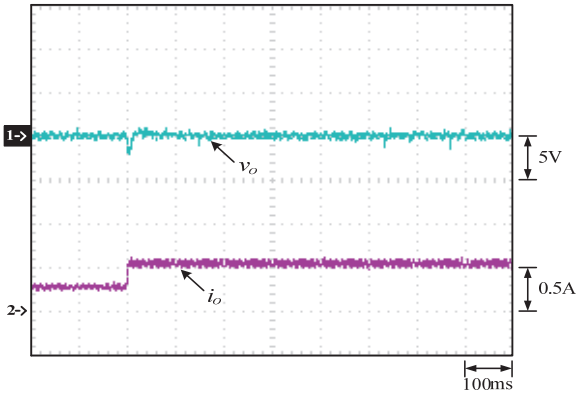

Fig. 36 Transient load response at 50% to 100% load.

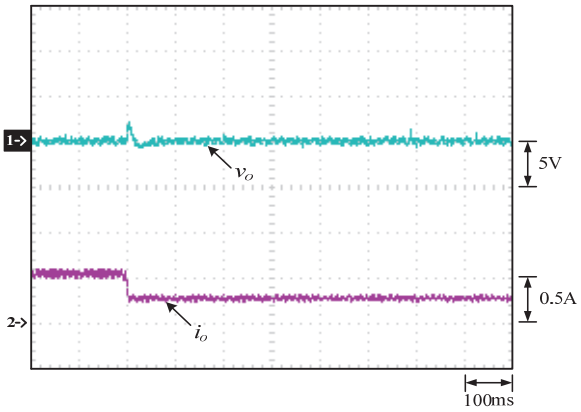

Fig. 37 Transient load response at 100% to 50% load.

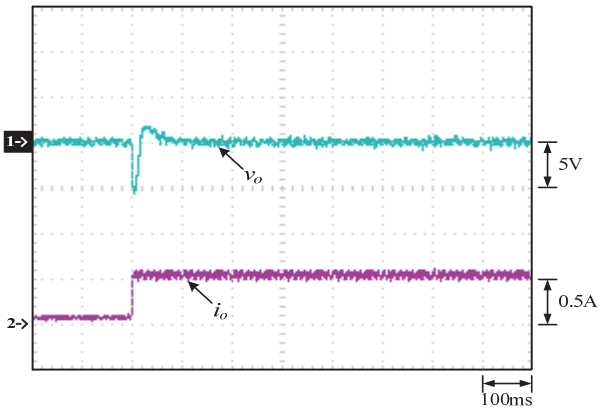

Fig. 38 Transient load response at 10% to 100% load.

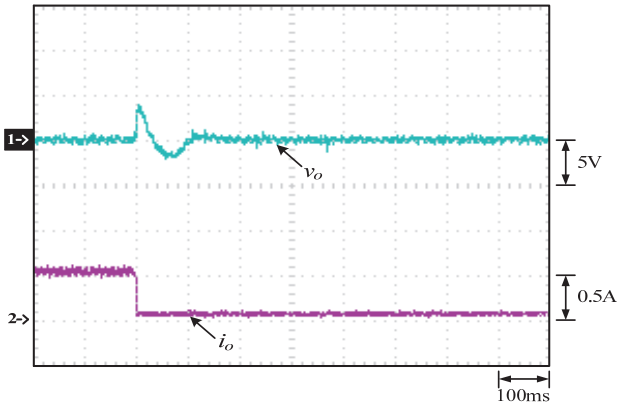

Fig. 39 Transient load response at 100% to 10% load.

4.3 Efficiency Curve and Loss Breakdown Analysis

Fig. 40 shows that the efficiency of the design across the entire load range exceeds 91.5%. Greatest efficiency is 97.2%, and the rated-load efficiency is 95.6%.

Fig. 41 displays the breakdown loss analysis of the proposed circuit at rated load. It shows that total component loss is about 7.28W, and actual measured loss was about 9.21W.

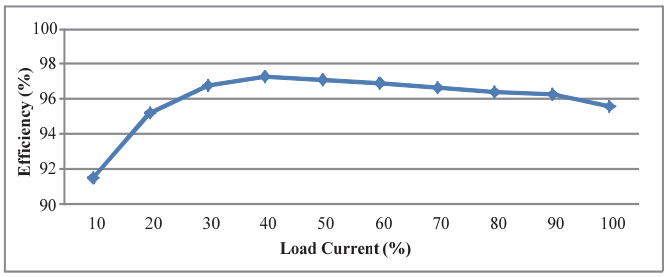

Fig. 40 Curve of load current vs efficiency.

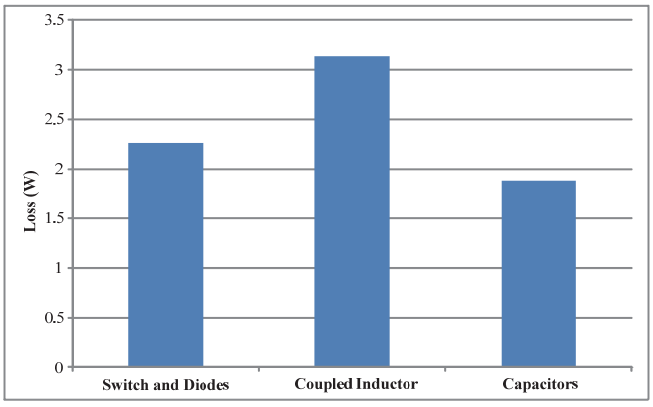

Fig. 41 Loss breakdown analysis.

4.4 Experimental Setup Photo

Figs. 42 and 43 display photos of a prototyped version of the proposed circuit, from the top and underside, respectively.

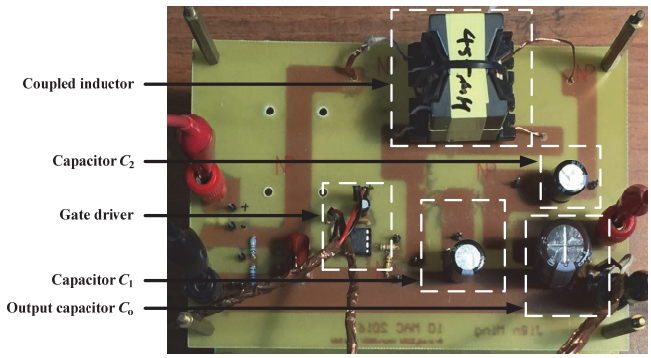

Fig. 42 Plan view of the prototype circuit.

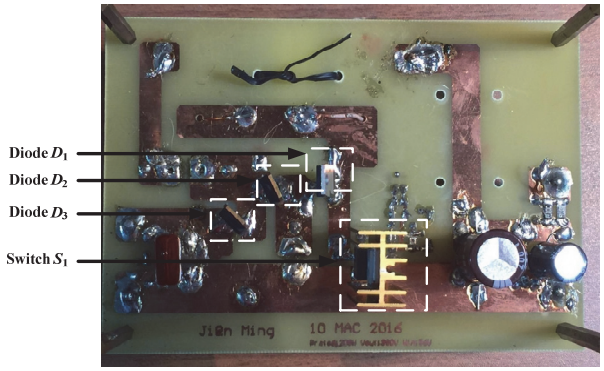

Fig. 43 Reverse side of the prototype circuit.

5. CONCLUSION

This manuscript first presented a theoretical design, and then tested a prototype of a novel, high step-up converter. Using coupling inductance and energy-transferring capacitors, this converter was able to achieve high step-up voltage gains, as well as recycle leakage inductance energy. The experimental results were promising, but some measured waveforms were different from the anticipated theoretical waveforms. Despite the different current slopes, the performance was still good, from the perspective of steady-state waveforms, transient waveforms and efficiency.

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