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Wide Voltage Range DC/DC Converter for Railway Auxiliary Power Units

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ABSTRACT

This paper proposes, manufactures and tests a universal DC power converter that uses a wide range of input voltages making it suitable as a power unit for railway trucks, or as an independent power management unit for stand-alone photovoltaic solar power systems. Due to variations in international standards for railway power units the nominal input voltage of a practical DC-DC converter should allow for a variation of at least 30% ~ 40%. However, the nominal input voltage of DC-DC converters for railway applications can be anything between 24V ~ 110V. Therefore, several DC converters with different nominal input voltages are required for differing railway transportation vehicles. To reduce the circuit count, this type of device acts as a universal DC converter. The hybrid DC converter includes a boost circuit under low voltage conditions and a full-bridge circuit to facilitate management of a wide input voltage range of 16V~160V. The boost circuit and full-bridge circuits operate under low input voltages to increase voltage gain. Where input voltage is high, only the full-bridge converter operates to provide stability of output. To validate the practicality of the proposed circuit, this paper ran experiments using a 420 W prototype.

Keywords: Wide voltage DC/DC converter, Phase-shift PWM, Soft switching operation.

1. INTRODUCTION

High speed rail vehicle techniques have technology has been developing rapidly in China due to the expansionist government policy and one belt one road strategy. High speed rail tucks and carriages require many types of power converter such as DC-AC for AC motor drives, and DC-DC converters for communication and control systems. The nominal input voltage of DC-DC converters on a railway system can be 24V, 37.5V, 48V, 72V, 96V or 110V, all of which are used for different purposes, from lighting, to electric door systems, motor drive controllers and braking systems. Compliance with the international standard EN50155, requires that an input voltage variation for DC-DC converters be greater than ±30% or ±40% of its nominal input voltage. For this reason engineers and researchers are focusing development on a universal DC-DC converter with a wide input voltage range to encompass nominal input voltages between 24 and 110V with ±30% voltage variation. Independent DC-DC power units for remote control systems are also required for stand-alone solar PV system. Howeversystems; however, the output voltage of solar cells varies greatly and depends heavily on solar luminance and geographical location. Therefore, a soft switching DC converter with a wide voltage range is also valuable for remote control systems on stand-alone solar power systems.

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DC converters with a wide input voltage operation were examined and then tested in solar power conversion and fuel-cell power conversion (*i.e.* electric vehicle charger) applications. A two-stage DC converter with buck, buck-boost or boost circuit topology was used in the front-stage and a push-pull, half-bridge or full-bridge circuit topology with fixed or variable frequency control was used in the rear-stage. These systems are established and have already been studied (Shang *et al*. 2015; Tong and Zhang 2016; Liya and Aathira 2104; Zhou *et al*. 2016; Jeong *et al*. 2017). Where the front-stage circuit is used to maintain the DC bus voltage at fixed value, and the rear-stage circuit operates at a fixed duty cycle to maintain the load voltage against load current variation. Since the front-stage circuit always operates under different input voltages, it is more challenging to optimize the circuit efficiency. Existing wide voltage range DC-DC converters with input-parallel output-parallel or series circuit topologies have been studied (Wang *et al*. 2017; Zhang *et al*. 2018; Balaji and Kowsalya 2017; Yao and Xu 2016); however the main problem with such topologies is the large number of components which reduces efficiency and reliability. Half-bridge or full-bridge converters with a phase-shift control on the secondary-side have been developed (Lu *et al*. 2018; Li *et al*. 2013, Shen *et al*. 2017; Wang *et al*. 2008; Wu *et al*. 2015) to encompass wide voltage operation, but the control algorithm on these circuits is too complex to be implemented by means of a general integrated circuit. Resonant circuits (Zong *et al*. 2018; Cha *et al*. 2010; Kim *et al*. 2018) have been developed to have a wide operational voltage range and high circuit efficiency. However, a review of the research on this topic shows that managing input voltage range by circuit topologies results in a ratio of less than 4:1, *i.e.* $V_{in,\,max} = 4V_{in,\,min}$. For solar power conversion applications DC-DC converters with a wider operational voltage range are required to overcome the vastly different input parameters caused by day and night cycles.

To attempt a remedy of this situation, a two-stage DC converter was developed that supports a wide operational input voltage range (10:1 input voltage range, 16V ~ 160V) and a soft switching operation. In the proposed converter, the front-stage is a boost circuit and the rear-stage is a full-bridge circuit. Compared to conventional two-stage DC-DC converters, the front-stage circuit only operates under low input voltages and is inactive during high input voltage periods. In the low voltage mode (5:1 voltage range, V_{in} = 16V ~ 80V), the boost circuit is used to provide a voltage boost-up, and the full-bridge converter at the rear-stage operates on a constant duty cycle to maintain circuit efficiency. In the high input voltage mode (1:1 voltage range, V_{in} = 80V ~ 160V), the boost circuit is bypassed and only the full-bridge converter is operational, working to control the load voltage and maintain circuit efficiency. In this approach, the proposed device can accept and manage a wide (10:1) input voltage range, and also decrease conduction loss and current ripple when operating in a high current (low voltage) side environment. This design uses a current-doubler rectifier topology, rather than a center-tapped rectifier topology. The rest of this paper discusses the circuit characteristics of the converter, testing of the prototype and finally the results of the experiment, which verify the effectiveness of the design.

2. CIRCUIT CONFIGURATION

Fig. 1(a) shows the structure of the prototype converter. The front-stage is a boost converter including components L_b, S_b, D_b and C_{BK}. The rear-stage is a full-bridge circuit, including the components $S_1 \sim S_4$, L_{lk}, T, SR_1, SR_2, L_{o1}, L_{o2} and C_o, that control the load voltage and manage the soft switching function. The synchronous switches SR_1 and SR_2 are employed on the high current (low voltage) side to decrease conduction loss over the power semiconductors. The current-doubler rectifier reduces output current ripple. According to the input voltage value, the proposed converter has two operation modes, low input voltage mode (Fig. 1(b)) and high input voltage mode (Fig. 1(c)). When input voltage $V_{in} = V_{in,\,min} \sim 5V_{in,\,min}$, the circuit operates in the low voltage mode, shown in Fig. 1(b). Both the boost circuit and full-bridge circuit are simultaneously functioning to control load voltage. Boost switch S_b is controlled by pulse-width modulation to boost the input voltage V_{in} and keep the DC bus voltage V_{BK} at the constant voltage $V_{BK,\,ref}$. The full-bridge circuit operates at a constant input voltage $V_{BK} = V_{BK,\,ref}$. Therefore, the duty cycle on the primary-side of the full-bridge is nearly constant and the root-mean-square current $i_{p,\,rms}$ is reduced, which reduces conduction loss on the power switches. When the input voltage is high and the circuit is running in high voltage mode ($V_{in} = 5V_{in,\,min} \sim 10V_{in,\,min}$) as shown in Fig. 1(c), the boost switch S_b is off and only the full-bridge circuit is operational, to manage the output voltage. This high/low input voltage switching function means that the device is suitable for the wide range of input voltages required for application in railway vehicles.

3. OPERATIONAL PRINCIPLE

Duty cycle modulation is used to produce a low, stable voltage output. According to the input voltage range, boost switch S_b will be in either an on or off position, yielding either the low ($V_{in,\,min} \sim 5V_{in,\,min}$) or high ($5V_{in,\,min} \sim 10V_{in,\,min}$) input voltage mode.

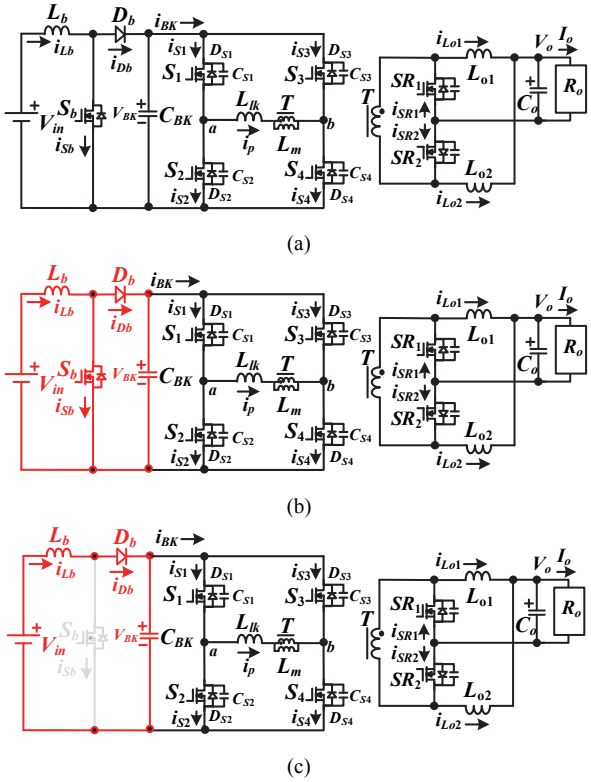


Fig. 1 Proposed 10:1 voltage range DC-DC converter (a) circuit structure, (b) equivalent circuit under low input voltages, (c) equivalent circuit under high input voltages.

A. *Low Input Voltage Mode*

When V_{in} is less than $5V_{in,\,min}$, both the boost and full-bridge circuits are operational (Fig. 1(b)). The boost converter regulates the maintain DC bus voltage $V_{BK} = V_{BK,\,ref}$. Boost switch S_b controls the voltage boost. The DC bus voltage V_{BK} is equal to V_{in} / (1-d_{Sb}) where d_{Sb} is the duty ratio of the switch S_b. Fig. 2(a) gives the main waveforms of the boost converter when it is in continuous conduction mode. The main features of the boost converter are to boost-up the voltage and ensure a continuous input current. Figs. 2(b) and 2(c) show the two operating steps that can be observed when the device is operating in continuous conduction mode.

Step 1 [$t_0 \le t < t_0 + d_{Sb}T_s$]: Boost switch S_b turns on at time t_0. The voltage across L_b is equal to V_{in} so that i_{Lb} increases. Buck capacitor C_{BK} discharges supplying power to the full-bridge converter through current i_{BK}. The voltage stress on the boost diode D_b equals V_{BK}.

Step 2 [$t_0 + d_{Sb}T_s \le t < t_0 + T_s$]: Boost switch S_b turns off at time $t_0 + d_{Sb}T_s$. In step 2, $v_{Lb} = V_{in} - V_{BK} < 0$, i_{Lb} decreases, $V_{Sb,\,ds} = V_{BK}$, D_b is forward biased and $i_{Db} = i_{Lb}$. Buck capacitor C_{BK} is charged from i_{Db}. At time $t_0 + T_s$, the boost converter goes to the next switching cycle.

For the full-bridge converter, the input voltage V_{BK} is constant and equal to $V_{BK,\,ref}$. Therefore, the effective duty cycle of the leg voltage v_{ab} is only related to load current. The waveforms of full-bridge converter are given in Fig. 3(a). There are ten equivalent steps in a switching period as shown in Figs. 3(b) ~ (k).

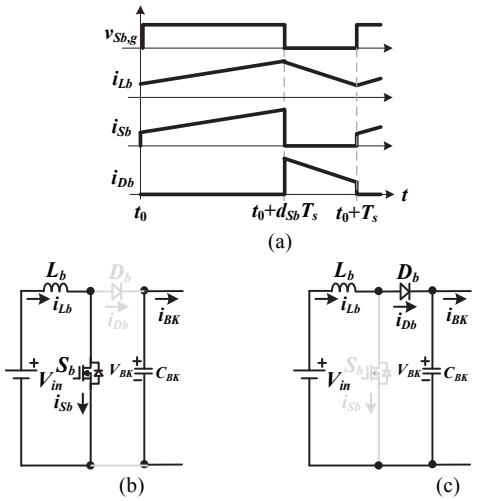
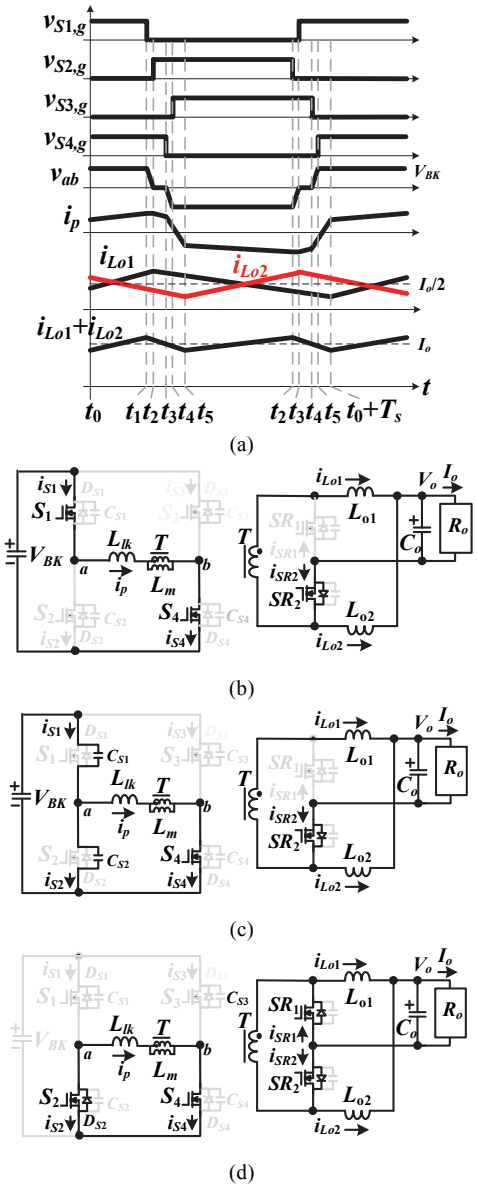


Fig. 2 **Boost converter performance under low input voltages (a) pulse-width modulation waveforms, (b) step 1 circuit, (c) step 2 circuit.**



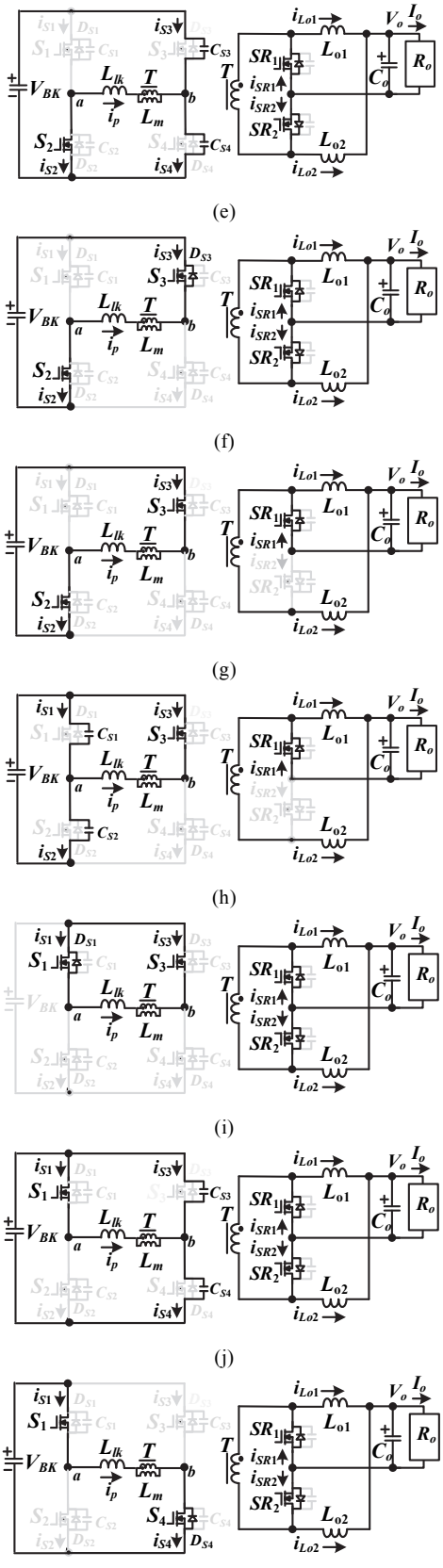


Fig. 3 **Prototype full-bridge converter circuit under low input voltages (a) pulse-width modulation waveforms, and circuit steps: (b) step 1, (c) step 2, (d) step 3, (e) step 4, (f) step 5, (g) step 6, (h) step 7, (i) step 8, (j) step 9, and (k) step 10.**

Step 1 [$t_0 \le t < t_1$]: In step 1, S_1 and S_4 are conducting so that $v_{Lm} \approx V_{BK}$. Input energy is delivered to secondary-side load through T, L_{o1}, Co and SR_2. The voltages across L_{o1} and L_{o2} are approximately calculated by $V_{BK}/n - V_o$ and $-V_o$, respectively where n is the turn ratio of transformer T. Therefore, i_{Lo1} increases and i_{Lo2} decreases.

Step 2 [$t_1 \le t < t_2$]: S_1 turns off at t_1. Owing to $i_p(t_1) > 0$, C_{S1} (C_{S2}) is linearly charged (discharged). Because C_{S1} and C_{S2} are low capacitances, the main currents are constant in step 2. The time interval in step 2 can be obtained by $\Delta t_{step\,2} \approx 2V_{BK}C_{oss}n/i_{Lo1}(t_1)$ where $C_{oss} = C_{S1} = .. = C_{S4}$.

Step 3 [$t_2 \le t < t_3$]: At t_2, $v_{CS2} = 0$ and $i_p > 0$ such that D_{S2} conducts and S_2 turns on, implementing zero voltage switching. The dead time t_d between S_1 and S_2 should follow equation (1) in order to have soft switching characteristics.

$$t_d > 2V_{BK}C_{oss}n / i_{Lo1}(t_1) \tag{1}$$

Because $L_{lk} << L_m$ and $R_{on,\,sw}$ (the turn-on resistance of the switch) are measured in hundredths of milliohms, the primary and secondary voltages of the transformer T are approximated at zero voltage. Thus, the body diodes of the synchronous switches SR_1 and SR_2 begin conducting. In order to reduce the conduction losses on the secondary-side (high current side), SR_1 and SR_2 are forced to turn on and $v_{Lo1} = v_{Lo2} = -V_o$. Thus, i_{Lo1} and $_{iLo2}$ decrease. The voltage drop ($V_{S,\,drop}$) on S_2 and S_4, and the primary current approximates to $i_p(t) \approx i_p(t_2) - V_{S,\,drop}/r_{lk}$, where r_{lk} is the equivalent series resistance on the leakage inductor L_{lk}.

Step 4 [$t3 \le t < t_4$]: S_4 turns off at t_3. Because $i_p(t_3) > 0$, C_{S3} (C_{S4}) is discharged (charged) by i_p. The main currents in the proposed circuit in this step are constant.

Step 5 [$t_4 \le t < t_5$]: $v_{CS3} = 0$ at t_4. Because of $i_p(t_4) > 0$, D_{S3} conducts and S_3 turns on to implement soft switching. In this step, both synchronous switch currents i_{SR1} and i_{SR2} are positive, $v_{Lm} = 0$ and $v_{ab} = -V_{BK}$. The leakage inductor voltage can be obtained as $v_{Llk} = -V_{BK}$ and i_p decreases from positive current $i_p(t_4)$ to negative current $i_p(t_5)$. The time duration in this step is calculated by:

$$\Delta t_{step\,5} = (i_p(t_4) - i_p(t_5))L_{lk} / V_{BK} \approx (I_o L_{lk}) / (nV_{BK}) \tag{2}$$

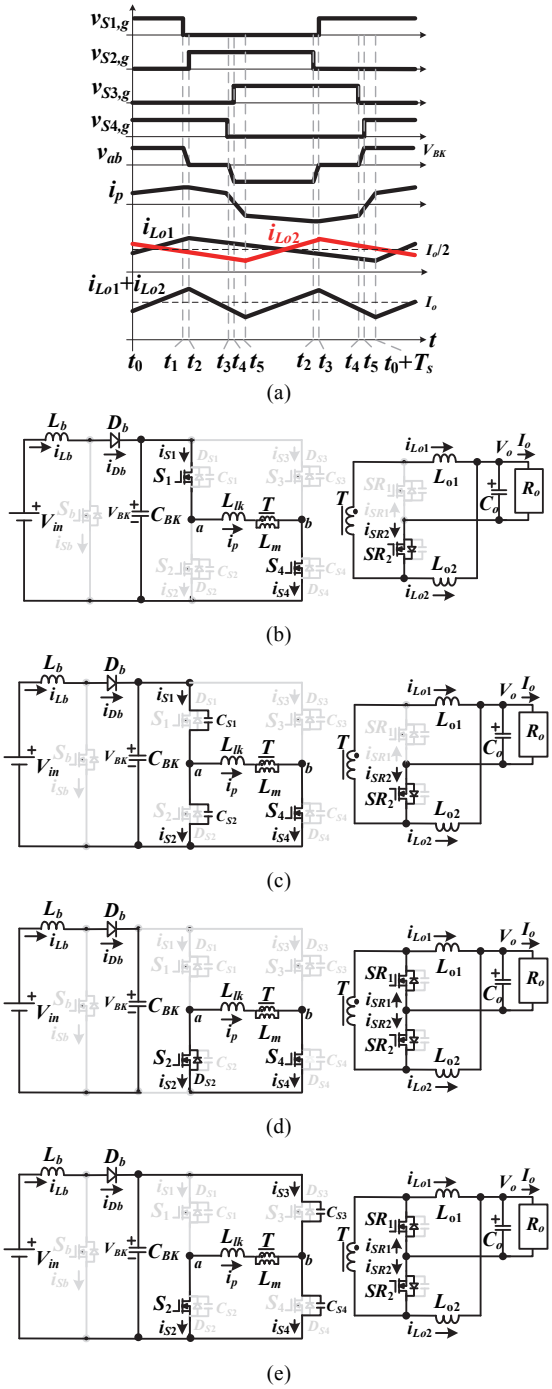
Because SR_1 and SR_2 are conducting and $v_{ab} = -V_{BK}$, no power is transferred to the secondary-side load. The duty cycle loss at step 5 is given by:

$$d_{loss,5} = \Delta t_{step\,5} / T_s \approx (I_o L_{lk} f_s) / (nV_{BK}) \tag{3}$$

At t_5, the synchronous switch current $i_{SR2} = 0$ and switch SR_2 is turned off. Owing to the voltage and current waveforms, steps 6 ~ 10 are symmetrical to the waveforms from steps 1-5. Thus, the circuit analysis and discussion of steps 6 ~ 10 will be omitted.

B. *High Input Voltage Mode*

When $5V_{in,\,min} < V_{in} \le 10V_{in,\,min}$, boost switch S_b is off and only a full-bridge converter is controlled during the high voltage mode (Fig. 1(c)). Under this condition, the DC bus voltage $V_{BK} = V_{in}$. The active devices $S_1 \sim S_4$ are gated to adjust the load voltage. The effective duty ratio depends on input voltage V_{in} and load current I_o. The minimum input voltage $V_{in} = 5V_{in,\,min}$ under the high voltage mode operation has a more effective duty cycle and the maximum input voltage $V_{in} = 10V_{in,\,min}$ has a less effective duty cycle. The main pulse-width modulation waveforms of the full-bridge converter in its high input voltage mode are shown in Fig. 4(a). The waveform difference between Fig. 3(a) (where V_{BK} is constant in the low input voltage setting) and Fig. 4(a) (where V_{BK} is not constant under the high input voltage setting) is only the effective duty cycle. The ten circuit operation steps (Figs. 4(b) ~ 4(k)) using the full-bridge converter in high voltage mode are similar to the circuit operations under low voltage inputs that were discussed in the previous section. For this reason the circuit discussion regarding the full-bridge circuit under high input voltage will be omitted from this section.



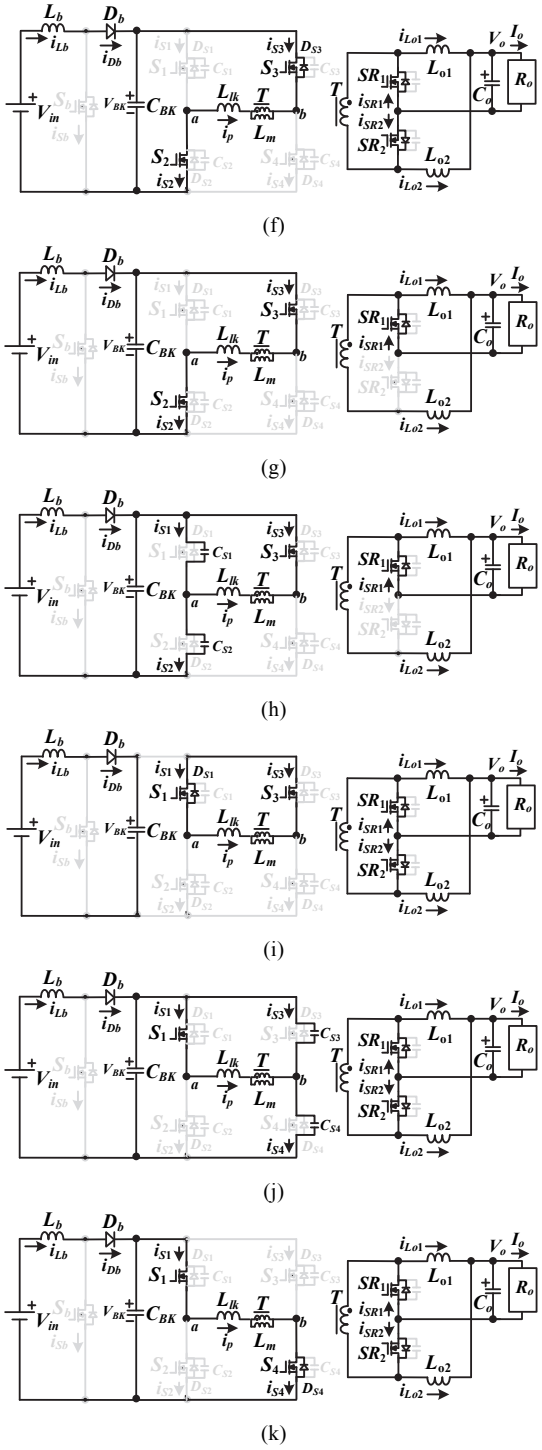


Fig. 4 Prototype converter operation in high input voltage mode showing (a) pulse-width modulation waveforms, and circuit (b) step 1, (c) step 2, (d) step 3, (e) step 4, (f) step 5, (g) step 6, (h) step 7, (i) step 8, (j) step 9, and (k) step 10.

4. CIRCUIT CHARACTERISTICS

Under the low input voltage conditions ($V_{in} = V_{in,\min} \sim 5V_{in,\min}$) the boost converter operates controlling the DC bus voltage $V_{BK} = V_{BK,ref}$. Where S_b is on, then $V_{Lb} = V_{in}$. Conversely, where S_b is off, $V_{Lb} = V_{in} - V_{bk}$. From the flux balance on boost inductor L_b under continuous conduction mode, the DC bus voltage V_{BK} is calculated by:

$$V_{BK} = V_{in} / (1 - d_{Sb}) \tag{4}$$

where d_{Sb} is the S_b duty cycle. Because $V_{in} = V_{in,\min} \sim 5V_{in,\min}$ under low input voltages, the necessary duty cycle d_{Sb} can be obtained by:

$$d_{Sb,min} = (V_{BK} - 5V_{in,min}) / V_{BK} \tag{5}$$

$$d_{Sb,max} = (V_{BK} - V_{in,min}) / V_{BK} \tag{6}$$

The *rms* current $I_{Sb,rms}$ is approximated by:

$$I_{Sb,rms} = I_{BK}\sqrt{d_{Sb}} / (1 - d_{Sb}) \tag{7}$$

Furthermore, the average and *rms* values of diode current can be approximated by:

$$I_{Db} = I_{BK} \tag{8}$$

$$I_{Db,rms} = I_{BK} / \sqrt{1 - d_{Sb}} \tag{9}$$

The *rms* value of the boost inductor current is calculated by:

$$I_{Lb,rms} = I_{BK} / (1 - d_{Sb}) \tag{10}$$

In the high input voltage mode, S_b is off, which means that the DC bus voltage V_{BK} is equal to the input voltage V_{in}.

The full-bridge converter can be controlled at constant input voltage by $V_{BK,ref}$ when in low input voltage mode, or variable input voltage $V_{BK} = V_{in}$ when in high input voltage mode. In low voltage mode, the duty cycle of leg voltage v_{ab} is about 0.5; however, this duty cycle depends on the input voltage V_{BK} when operating in high voltage mode. The phase-shift technique is used to control load voltage between the leading-leg and lagging-leg. According to the flux balance on L_{o1} or L_{o2}, the load voltage V_o can be approximated by:

$$V_o = \frac{V_{BK}}{n}\left(d - \frac{L_{lk} I_o f_s}{n V_{BK}}\right) \tag{11}$$

where d is the duty cycle of v_{ab}. In this prototype, the selected primary turns were $n_p \geq V_{BK} dT_s / (\Delta B_{\max} A_e)$ where $\Delta B_{\max}$ was the flux density variation and A_e was the effective cross area of the core, with secondary turns of $n_s = n_p / n$. The average values of the output inductor currents i_{Lo1} and i_{Lo2} were equal to $I_o / 2$ in a steady state condition. The voltage stress of the active devices $S_1 \sim S_4$ were equal to $V_{BK,\max} = V_{in}$, max under high input voltage mode. The voltage rating of the synchronous switches S_{R1} and S_{R2} equal $V_{BK,\max}/n$. If the ripple current $\Delta i_{Lo1} = \Delta i_{Lo2} = \Delta i_{Lo}$ is given, then L_{o1} and L_{o2} can be approximated by:

$$L_o = \frac{V_o}{\Delta i_{Lo} f_s}\left(1 + \frac{L_{lk} I_o f_s}{n V_{BK}} - d\right) \tag{12}$$

Where the duty loss is known, the leakage inductance L_{lk} can be approximated by:

$$L_{lk} = \frac{nV_{BK}d_{loss,5}}{I_o f_s} \tag{13}$$

5. EXPERIMENTAL RESULTS

The presented DC-DC converter was developed into to a laboratory prototype with V_{in} = 16V ~ 160V (10:1 ratio), V_o = 12V, I_o, rated = 35A and f_s = 100 kHz. Where V_{in} = 16V ~ 76V (low voltage mode), the boost and full-bridge converters operated to control the DC bus voltage V_{BK} = 80V and load voltage V_o = 12V. Where V_{in} = 75V ~ 160V (high voltage mode), only the full-bridge converter controlled the output voltage V_o = 12V. In low voltage mode, the switch S_b was controlled to achieve the voltage boost and make V_{BK} = 80V. Thus, the duty cycle of switch S_b can be calculated by:

$$d_{Sb,min} = \frac{V_{BK} - V_{in,max}}{V_{BK}} = \frac{80-76}{80} = 0.05 \tag{14}$$

$$d_{Sb,max} = \frac{V_{BK} - V_{in,min}}{V_{BK}} = \frac{80-16}{80} = 0.8 \tag{15}$$

It is assumed that the designed ripple current Δi_{Lb} is about 8A at 16V input. The boost inductance L_b is thus calculated by:

$$L_b = \frac{V_{in,min}d_{Sb,max}}{\Delta i_{Lb} f_s} = \frac{16\times 0.8}{8\times 10^5} = 16\ \mu H \tag{16}$$

The *rms* value of i_{Sb} and the average value of i_{Db} are given by:

$$I_{Sb,rms} = \frac{I_{BK}\sqrt{d_{Sb,max}}}{1-d_{Sb,max}} = \frac{(420/80)\sqrt{0.8}}{1-0.8} \approx 23.5A \tag{17}$$

$$I_{Db} = I_{BK} = 420/80 = 5.25A \tag{18}$$

The MOSFET IRFB260N with 200V/56A rating was used for the boost switch S_b and the fast recovery diode MBR40200PT with a 200V/40A rating was used for the boost diode D_b.

The circuit efficiency of the full-bridge converter at full power was assumed to be 92%. It is assumed that the maximum duty cycle of leg voltage v_{ab} at V_{BK} = 75V is 0.48 and the duty cycle loss $d_{loss,5}$ is less than 0.04.

$$d_{loss,5} = (I_o L_{lk} f_s)/(nV_{BK}) < 0.04 \tag{19}$$

The maximum leakage primary inductor is calculated by:

$$L_{lk} < \frac{\eta d_{loss,5}\, d_{max}V_{BK,min}^2}{P_o f_s} \approx 2.4\mu H \tag{20}$$

From (11), the turn-ratio n is approximated by:

$$n \approx \frac{d_{max}V_{BK,min} + \sqrt{(d_{max}V_{BK,min})^2 - 4V_o L_{lk} I_o f_s}}{2V_o} \approx 2.75 \tag{21}$$

The TDK EER-42 ferrite core was used as the transformer T with winding turns n_p = 22 and n_s = 8 and L_m = 300μH. It was assumed that the maximum ripple currents $\Delta I_{Lo1,\max}$ = $\Delta I_{Lo2,\max}$ = 5A at maximum DC bus voltage V_{BK} = 160V. The minimum effective duty cycle $d_{eff,min}$ at V_{BK} = 160V can thus be approximated by:

$$d_{eff,min} = \frac{d_{eff,max}V_{BK,min}}{V_{BK,max}} = \frac{(048-0.04)\times 75}{160} \approx 0.206 \tag{22}$$

Therefore, the inductances Lo_1 and Lo_2 are approximated by:

$$L_{o1} = L_{o2} \approx \frac{(V_{BK,max}/n - V_o)d_{eff,min}}{\Delta i_{Lo1} f_s} = 19\mu H \tag{23}$$

The *rms* values of $S_1 \sim S_4$, SR_1 and SR_2 are approximated by:

$$I_{S1,rms} = .. = I_{S4,rms} \approx \frac{I_o}{2n\eta\sqrt{2}} \approx 4.9\text{A} \tag{24}$$

$$I_{SR1,rms} = I_{SR2,rms} \approx \frac{I_o}{\sqrt{2}} \approx 24.7\text{A} \tag{25}$$

The voltage ratings for $S_1 \sim S_4$, SR_1 and SR_2 can be obtained by:

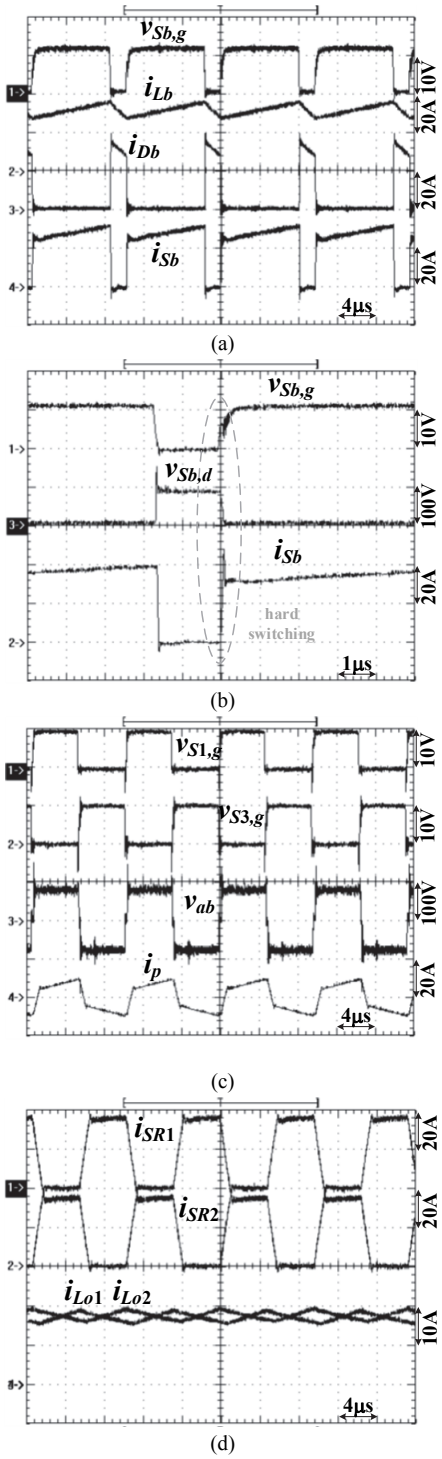
$$V_{S1,rating} = .. = V_{S4,rating} = V_{BK,max} = 160\text{V} \tag{26}$$

$$V_{SR1,rating} = V_{SR2,rating} = V_{BK,max}/n \approx 58\text{V} \tag{27}$$

The MOSFET IRFB4229 with a 250V/46A rating was used for the active devices $S_1 \sim S_4$, and the IRFB4110 with a 100V/180A rating was used for the synchronous switches SR_1 and SR_2.

Figs. 5 and 6 provide the experimental waveforms of the presented circuit in low voltage mode (V_{in} = 16V ~ 76V). Fig. 7 gives the experimental waveforms in high voltage mode (V_{in} = 75V ~ 160V). In the low input voltage mode, both boost circuit and full-bridge circuit produced V_{BK} = 80V and V_o = 12V. The experimental waveforms under the 16V input case are presented in Fig. 5. The experimental waveforms i_{Lb}, i_{Sb} and i_{Db} for the rated power are shown in Fig. 5(a). Fig. 5(b) shows the experimental results of switch S_b at full load. It can be seen that S_b operates as a hard switch for instances of switching both on and off. The measured gate voltages $v_{S1,g}$ (at leading-leg) and $v_{S3,g}$ (at lagging-leg), leg voltage vab and primary-side current i_p at rated power are provided in Fig. 5(c). Since the DC bus voltage V_{BK} was controlled at 80V under the low input voltage mode, the duty cycle of leg voltage v_{ab} was approximately 0.5. The measured secondary-side currents i_{SR1}, i_{SR2}, i_{Lo1}, i_{Lo2} and i_{Lo1} + i_{Lo2} at rated power were provided in Figs. 5(d) and 5(e). The current ripples on L_{o1} and L_{o2} were partially eliminated and the *rms* value of i_{Lo1} + i_{Lo2} were reduced. Fig. 5(f) exhibits the S_1 leading-leg waveforms at 15% of rated power. It can be seen that S_1 turns on with zero-voltage switching at 15% rated power. S_2 has the same on/off characteristics as S_1. In the same way, the test results of the S_3 lagging-leg at 40% load are shown in Fig. 5(g). From the

test results, the zero-voltage switching of S_3 occurs at 40% of load. S_4 has the same on/off characteristics as S_3. Fig. 6 shows the test results under a 76V input (low input voltage mode). Fig. 6(a) provides the waveforms of the boost converter at its rated load. Since 76V input voltage is very close to the DC bus voltage V_{BK} = 80V, the duty cycle of S_b is approximately 0.05. Fig. 6(b) shows the test results of the switch S_b at full power. It is clear that the boost switch S_b turns on under hard switching. Since V_{BK} = 80V for both 16V and 76V input cases, the measured waveforms of the full-bridge converter shown in Figs. 6(c) ~ 6(g) under the 76V input case are similar to results seen in Figs. 5(c) ~ 5(g) for the 16V case.



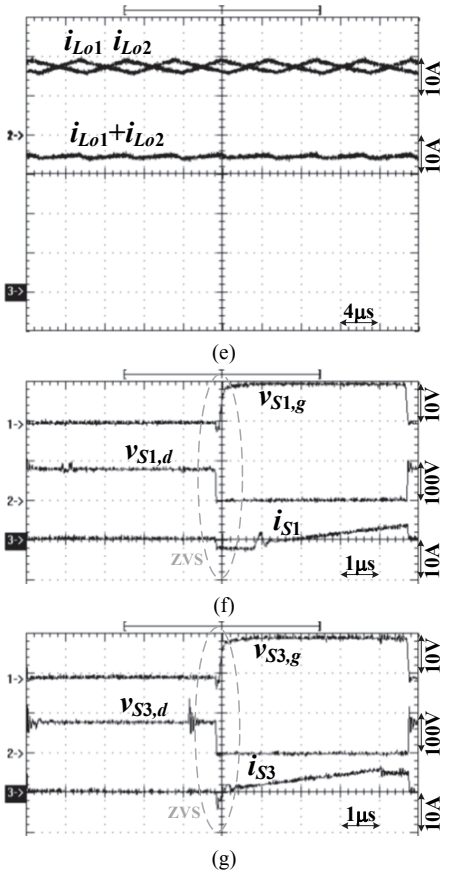
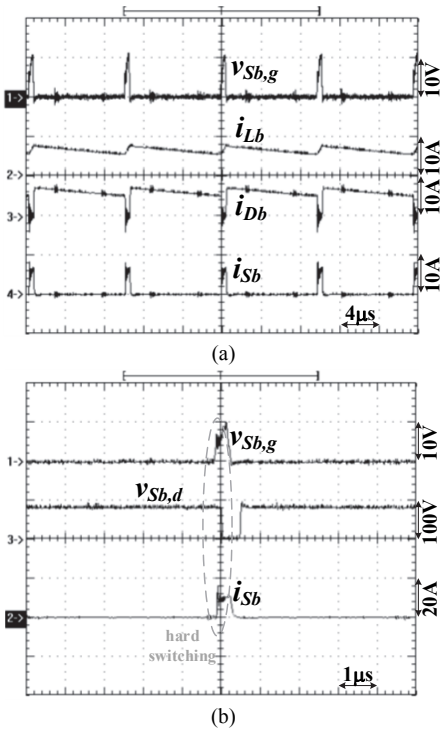


Fig. 5 Laboratory observations where V_{in} = 16V (low voltage mode) and (a) $v_{Sb,g}$, i_{Lb}, i_{Sb}, i_{Db} at rated power, (b) $v_{Sb,g}$, $v_{Sb,d}$, i_{Sb} at rated power, (c) $v_{S1,g}$, $v_{S3,g}$, v_{ab}, i_p at rated power, (d) i_{SR1}, i_{SR2}, i_{Lo1}, i_{Lo2} at rated power, (e) i_{Lo1}, i_{Lo2}, $i_{Lo1} + i_{Lo2}$ at rated power, (f) $v_{S1,g}$, $v_{S1,d}$, i_{S1} at 15% rated power, and (g) $v_{S3,g}$, $v_{S3,d}$, i_{S3} at 40% rated power.



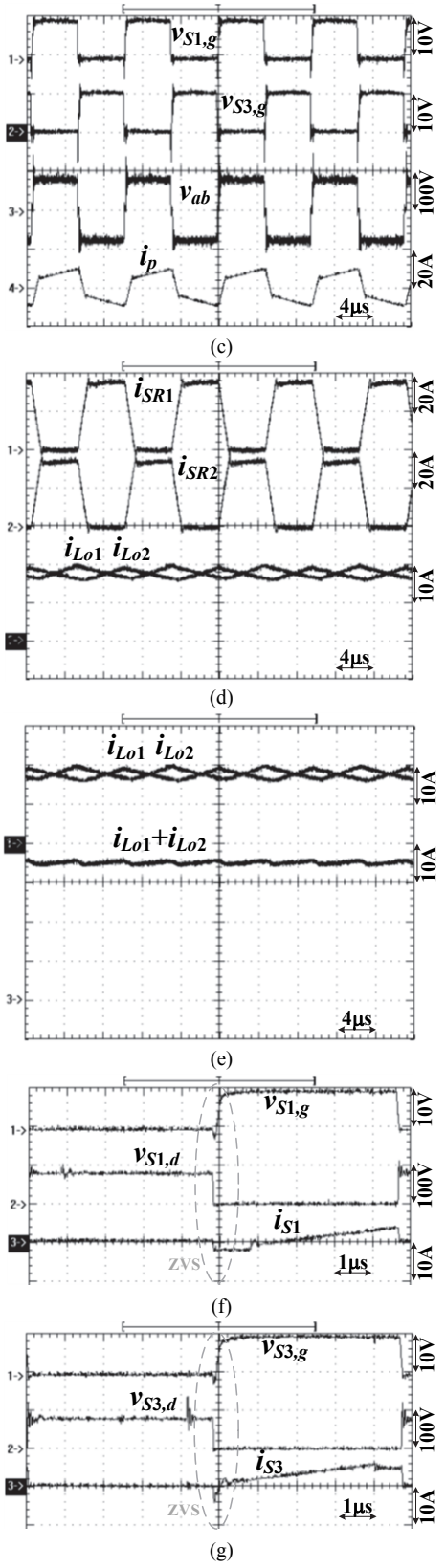
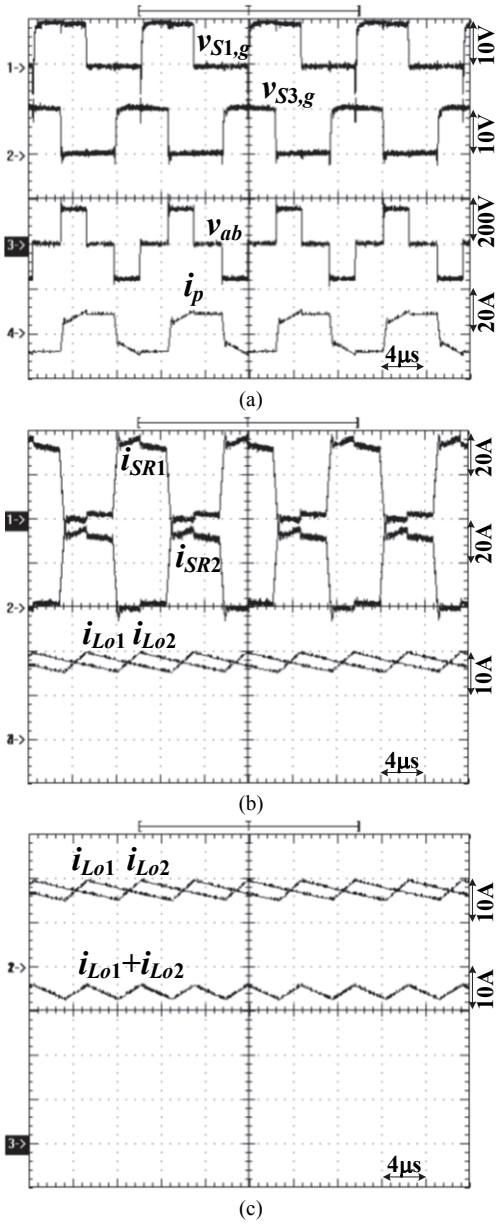
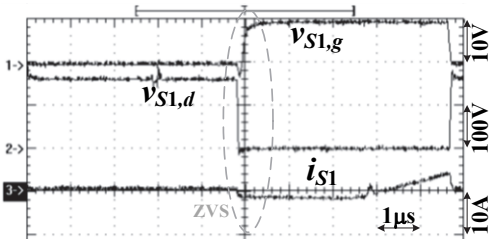


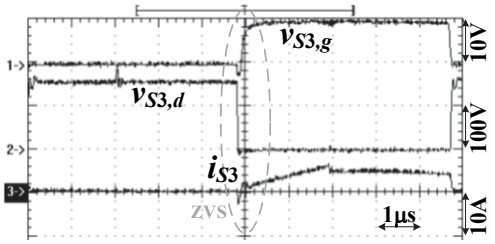
Fig. 6 Laboratory observations where V_{in} = 76V (low voltage mode) and (a) $v_{Sb,\,g}$, i_{Lb}, i_{Sb}, i_{Db} at rated power, (b) $v_{Sb,\,g}$, $v_{Sb,\,d}$, i_{Sb} at rated power, (c) $v_{S1,\,g}$, $v_{S3,\,g}$, v_{ab}, i_p at rated power, (d) i_{SR1}, i_{SR2}, i_{Lo1}, i_{Lo2} at rated power, (e) i_{Lo1}, i_{Lo2}, i_{Lo1} + i_{Lo2} at rated power, (f) v_{S1}, g, $v_{S1,\,d}$, i_{S1} at 15% rated power, and (g) $v_{S3,\,g}$, $v_{S3,\,d}$, i_{S3} at 40% rated power.

Fig. 7 exhibits the measured waveforms at V_{in} = 160V (high voltage mode operation) and rated load. Under high voltage operation, boost switch S_b is off. Figs. 7(a) ~ 7(c) show the primary and secondary waveforms. Owing to the DC bus voltage V_{BK} = V_{in} under high voltage mode operation, the phase shift between leading and lagging-leg is controlled to regulate the voltage load. The duty cycle of v_{ab} is at its maximum (minimum) at V_{in} = 75V (160V). Therefore, in that circumstance the measured voltage v_{ab} is a quasi-square waveform. Figs. 7(d) and 7(e) show the test results of S_1 and S_3 at 15% and 40% of rated power, respectively. Based on the measured waveforms, both S_1 and S_3 achieved soft switching between 15% and 40% of rated power. Fig. 8 provides the circuit efficiencies under different conditions. It can be observed that the minimum input voltage V_{in} = 16V has the lowest efficiency due to the high conduction losses caused by powered devices. For the V_{in} = 80V case, the converter showed highest efficiency due to the maximum duty cycle of the leg voltage across the full-bridge circuit, and also because the boost switch S_b was off.





(d)



(e)

Fig. 7 Laboratory observations where V_{in} = 16V (high voltage mode) and (a) $v_{S1,g}$, $v_{S3,g}$, v_{ab}, i_p at rated power, (b) i_{SR1}, i_{SR2}, i_{Lo1}, i_{Lo2} at rated power, (c) i_{Lo1}, i_{Lo2}, $i_{Lo1}+i_{Lo2}$ at rated power, (d) $v_{S1,g}$, $v_{S1,d}$, i_{S1} at 15% rated power, and (e) $v_{S3,g}$, $v_{S3,d}$, i_{S3} at 40% rated power.

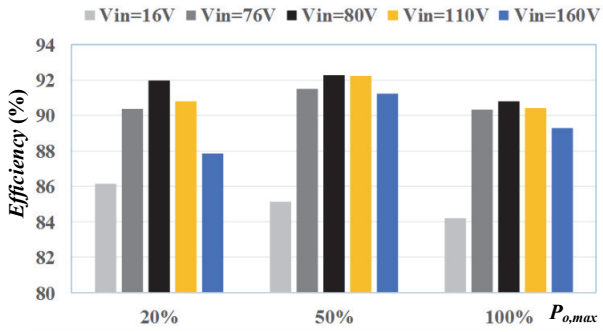


Fig. 8 Measured efficiencies under various conditions.

6. CONCLUSIONS

A wide voltage range DC converter was discussed, and manufactured for experimentation. The purpose of the device would be to serve as a railway vehicle power unit or independent power management unit for stand-alone photovoltaic solar power systems, which both typically require a wide operational input voltage range.

Input voltage range was detected in order to activate (or deactivate) the boost switch during low (or high) input voltage situations. When operating in the high input voltage mode, the boost switch is off and only the full-bridge circuit operates. Thus, the power conduction loss across the whole device can be reduced. The main contributions of this paper are: 1) The circuit operation and system analysis were provided for both low and high input voltage modes; 2) the circuit characteristics of the studied converter were discussed; and 3) an example of the prototype circuit using a 420W rated power supply were presented. The phase-shift technique was used to realize zero-voltage switching for the power switches on a full-bridge converter. The current-doubler rectifier with synchronous switches was adopted to decrease conduction loss across the power devices, and current ripple on the output inductor and capacitor. The performance and practicality of the converter are proven by the test results.

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