Journal of Innovative Technology, Vol. 4, No. 2, pp. 29-40, September 2022
http://doi.org/10.29424/JIT.202209_4(2).0004

High Voltage-Boosting Converter

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ABSTRACT

A high step-up converter, derived from the KY boost converter along with the coupled inductor and is used to improve the voltage conversion ratio of the KY boost converter. At the same time, the energy stored in the leakage inductance of the coupled inductor can be recycled. In the paper, the basis operating principles and mathematical deductions of the proposed converter are described in detail, and sequentially some simulated and experimental results are provided to verify the feasibility and effectiveness of such a converter. In addition, the filed-programmable gate array (FPGA), named EP1C3T100C8N made by Altera Co., is used as a system control kernel.

Keywords: Charge pump capacitor, coupled inductor, high voltage-boosting converter

1. INTRODUCTION

Nowadays, most countries need to use large-scale construction methods for power generation, such as thermal, nuclear, and hydroelectric power generation, to obtain the electricity needed for living. Although these methods have the advantage of being cheaper, they are often limited by their locations, such as thermal power generation, which is located far away from cities to prevent air pollution, hydroelectric power generation, which locates in places with water sources, and nuclear power generation, which must be located at the seaside to be cooled by seawater. Therefore, the above-mentioned power generation methods must be located far away from cities. In the past, the cost of setting up these large-scale power generation plants was very high, but in recent years, due to the improvement of the reliability of power generation, the cost of setting up plants has become lower than the cost of maintaining the power grid. There are several types of decentralized power generation, such as waste heat generation, solar power generation, electric vehicle-to-grid power generation, and wind power generation. In addition, the output voltage tends to change with the change of load. To solve this problem, a step-up converter is connected at the back end of the decentralized energy source to provide a relatively stable high voltage for the back-end equipment, or to provide the input power for the inverter of the utility grid system. For example, in thermo electrical generator (TEG), stand-alone solar power system (Gules et al., 2008), and utility-connected solar power system (Wu & Shen, 2010), a step-up converter is required to step up the low voltage generated by the thermoelectric module or solar panel to a high voltage to provide power to the inverter or load side.

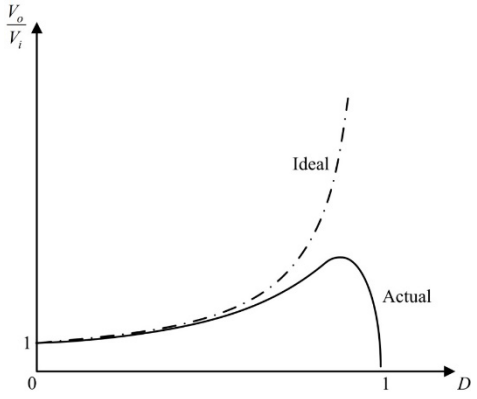

Fig. 1 Voltage conversion ratio versus duty cycle for the conventional boost converter.

In general, the voltage conversion ratio of the conventional boost converter is theoretically infinite, but due to the limitation of parasitic components, the voltage conversion ratio can only be increased to about four times, as shown in Fig. 1 (Erickson & Maksomovic, 2001).

Therefore, many novel step-up converters have been proposed, such as the KY converter and its related derivatives (Hwu & Yau, 2009, 2010; Hwu, Huang & Tu, 2011; Hwu & Jiang, 2014), which operate on a simple charge pump circuit with either a step-up inductor or a coupled inductor to obtain a high voltage conversion ratio. In contrast, the references (Hwu & Yau, 2011; Hwu, Chuang & Tu, 2012; Hwu & Tu, 2012) use a charge pump circuit with single or multiple magnetic elements to improve the voltage conversion ratio. In Li et al. (2010), Tseng, Huang & Shih (2013), Lai, Pan & Cheng (2012), and Zhou, Zhu & Luo (2012), an interleaved boost circuit is proposed to reduce the high input current, and the main principle is to use coupled inductors to achieve a high voltage conversion ratio. In Chen et al. (2013), Hu & Gong (2014), Pan & Lai (2010), Hwu, Yau & Shieh (2013), Hsieh et al. (2011A), Chen et al. (2013A), Chen et al. (2012), Zhao et al. (2013), Zhao et al. (2011), Wai & Duan (2005), Laird & Lu (2013), Hsieh et al. (2014), Wai & Jheng (2013), Zhao & Lee (2003), Hsieh et al. (2013), Hsieh et al. (2011B), Yang et al. (2011), Liang et al.

Manuscript received June 23, 2022; revised June 30, 2022; accepted July 5, 2022.

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(2013), Deng et al. (2012), Lee, Liang & Chen (2014) and Evran & Aydemir (2013), coupled inductors are used with either a voltage doubler or a switched capacitor to achieve high voltage conversion ratios. In Chen et al. (2011), Chu, Lu & Agelidis (2012), Park, Moon & Youn (2010, 2011, 2012), and Changchien et al. (2010), coupled inductors with voltage doublers or switched capacitors are used to obtain higher voltage conversion ratio.

Compared with the conventional boost converters, all the above-mentioned structures have higher voltage conversion ratios, but each has its own drawbacks. In Hwu & Yau (2009, 2010), Hwu, Huang & Tu (2011) and Hwu & Yau (2012), although the structures are simple and easy to implement, the voltage conversion ratios are still not high enough. In Hwu & Yau (2009, 2010), Hwu, Huang & Tu (2011), Hwu & Jiang (2014), Hwu, Chuang & Tu (2014), Hwu & Tu (2012), Chen et al. (2013), Hwu, Yau & Shieh (2013), Chen et al. (2012), Zhao et al. (2013), Hsieh et al. (2014), Yang et al. (2011) and Liang et al. (2013), the converter has floating switches, which require an additional isolation gate drivers and increase the converter cost. In Hwu, Chuang & Tu (2014), Lai, Pan & Cheng (2012) and Deng et al. (2012), too many components make the design difficult and costly. In Hwu & Jiang (2014), Chen et al. (2013A), Chen et al. (2013), Chen et al. (2012) and Hsieh et al. (2014), the converter uses the turns ratio of the coupling inductor to increase the voltage conversion ratio, but the coupling inductor has the problem of leakage inductance, which tends to resonate with the parasitic capacitance of the switch or diode, thus causing excessive voltage spike on the switch or diode. Therefore, it is necessary to select components with higher rated voltage withstand or add additional buffers to overcome this drawback, thereby making the circuit implementation difficult. Multiple voltage doubling circuits are used to achieve higher voltage conversion ratios, thereby increasing the number of diodes and capacitors and leads to higher costs and more complex designs, as shown in Tseng, Huang & Shih (2013), Hu & Gong (2014), Pan & Lai (2010), Hwu, Yau & Shieh (2013), Hsieh et al. (2011A), Chen et al. (2012), Zhao et al. (2013), Hsieh et al. (2014), Hsieh et al (2013), Hsieh et al. (2011), Liang et al. (2013), Evran & Aydemir (2013), Park, Moon & Youn (2011, 2012), and Changchien et al. (2010).

Hence, the proposed high voltage-boosting converter is presented, which is derived from the KY boost converter along with the input inductor coupled with the output inductor to upgrade the voltage conversion ratio.

2. KY BOOST CONVERTER

The proposed high voltage-boosting converter is derived from the KY boost converter. Therefore, we will first introduce the basic operation principle of KY boost converter and its related mathematical derivation.

Fig. 2 shows the circuit architecture of the KY boost converter. The circuit consists of two inductors L_i and L_o, one diode D_1, two energy-transferring capacitors C_1 and C_2, two switches S_1 and S_2 and one output capacitor C_o. As for the output load, it is expressed in terms of resistance R_o.

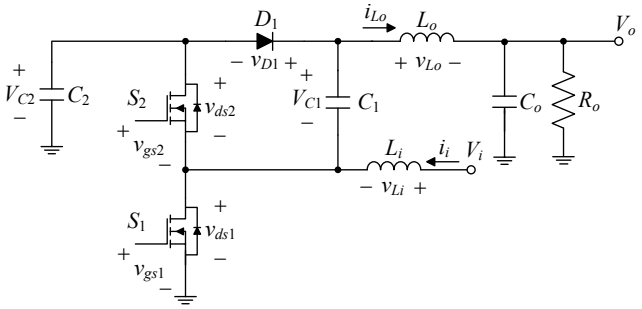

Fig. 2 KY boost converter.

Before analyzing the circuit operation, a brief explanation of the relevant symbols and their required assumptions is provided: (i) the input voltage is V_i and the output voltage is V_o; (ii) the values of the energy-transferring capacitors and output capacitor are large enough to have certain values across them; (iii) the switching frequency is f_s; (iv) all the switches, diodes, and capacitors are considered ideal components; (v) the driving signal for the switch S_1 and the driving signal for the switch S_2 are complementary; and (vi) the circuit is operated in the continuous conduction mode (CCM), with two operating states over one switching cycle as shown in Fig. 3.

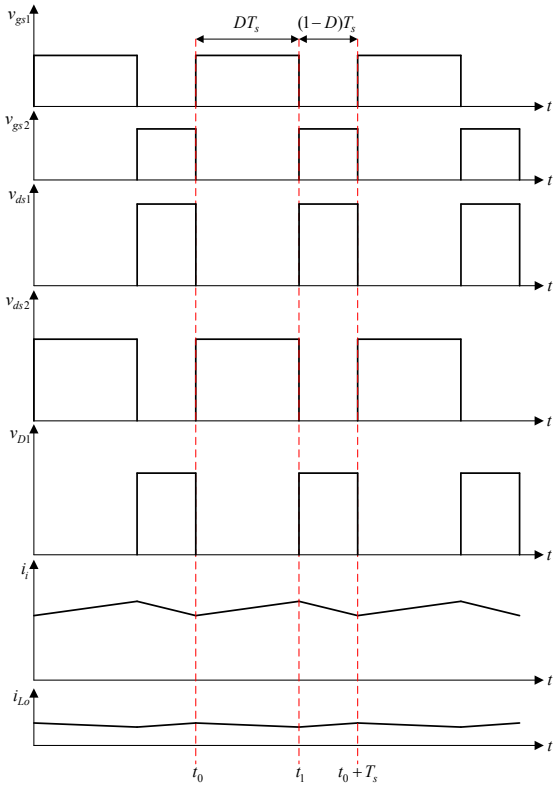

Fig. 3 Illustrated waveforms relevant to the KY boost converter operating.

State 1: $[t_0 \leq t \leq t_1]$

The switch S_1 is on and the switch S_2 is off, and the diode D_1 is on, as shown in Fig. 4. At the same time, the voltage across the inductor L_i is the input voltage V_o, so it is in the magnetization

state; the voltage across the inductor L_o is the voltage across the energy-transferring capacitor V_{C1} minus the output voltage V_o, so it is in the demagnetization state. In addition, the energy-transferring capacitor C_2 charges the energy-transferring capacitor C_1 and transfers energy to the load.

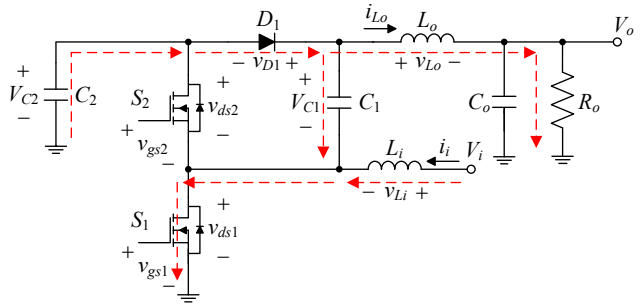

Fig. 4. Current flow of state 1.

State 2: $[\, t_1 \le t \le t_2 \,]$

The switch is S_1 turned off and the switch S_2 is turned on, and the diode D_1 is turned off, as shown in Fig. 5. At the same time, the voltage across the inductor L_i is the input voltage V_i minus the voltage across the energy-transferring capacitor C_2, so it is in the demagnetization state and charging the energy-transferring capacitor C_2; the voltage across the inductor L_o is the voltage across the energy-transferring capacitor C_1 plus the voltage across the energy-transferring capacitor C_2 minus the output voltage V_o, so it is in the magnetization state, and, together with the input voltage, the inductor L_i and the energy-transferring capacitor C_1, provides the energy for the load.

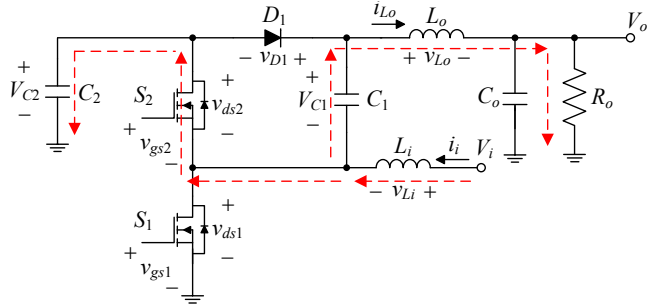

Fig. 5 Current flow of state 2.

The equation corresponding to state 1 can be found from Fig. 4 to be

$$\begin{cases} v_{Li} = V_i \\ v_{Lo} = V_{C1} - V_o \end{cases} \tag{1}$$

The equations corresponding to state 2 can be found from Fig. 5 as

$$\begin{cases} v_{Li} = V_i - V_{C1} \\ v_{Lo} = V_{C1} + V_{C2} - V_o \end{cases} \tag{2}$$

Also,

$$V_{C1} = V_{C2} \tag{3}$$

Therefore, (3) can be rewritten as

$$\begin{cases} v_{Li} = V_i - V_{C1} \\ v_{Lo} = 2V_{C1} - V_o \end{cases} \tag{4}$$

By using the voltage on the inductor to meet the volt-second balance in the steady state, we can obtain

$$V_i D + (V_i - V_{C1})(1-D) = 0 \tag{5}$$

$$(V_{C1} - V_o)D + (2V_{C1} - V_o)(1-D) = 0 \tag{6}$$

Rearranging (5) yields

$$\frac{V_{C1}}{V_i} = \frac{1}{1-D} \tag{7}$$

Then, by bringing (7) into (6), we obtain

$$\frac{V_o}{V_i} = \frac{2-D}{1-D} \tag{8}$$

3. PROPOSED HIGH VOLTAGE-BOOSTING CONVERTER

Fig. 6 displays the proposed high voltage-boosting converter. This circuit consists of two switches S_1 and S_2 and one diode D_1, two energy-transferring capacitors C_1 and C_2, and one coupled inductor consisting of one primary winding N_p, one secondary winding N_s and one magnetizing inductor L_m, one output diode D_o and one output capacitor C_o, and as for the output load, it is expressed in terms of resistance R_o.

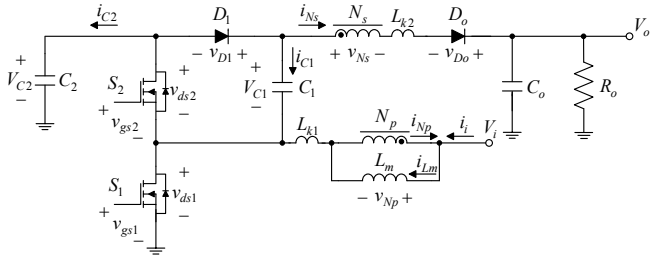

Fig. 6 Proposed high voltage-boosting converter.

Before analyzing the circuit operation, a brief explanation of the relevant symbols and their required assumptions is provided: (i) the input voltage is V_i and the output voltage is V_o; (ii) the values of the energy-transferring capacitors and output capacitor are large enough to have certain values across them; (iii) the switching frequency is f_s; (iv) all the switches, diodes, and capacitors are considered ideal components; (v) the driving signal of the switch S_1 and the driving signal of the switch S_2 are complementary; and

(vi) the circuit is operated in the continuous conduction mode (CCM), with five operating states over one switching cycle as shown in Fig. 7.

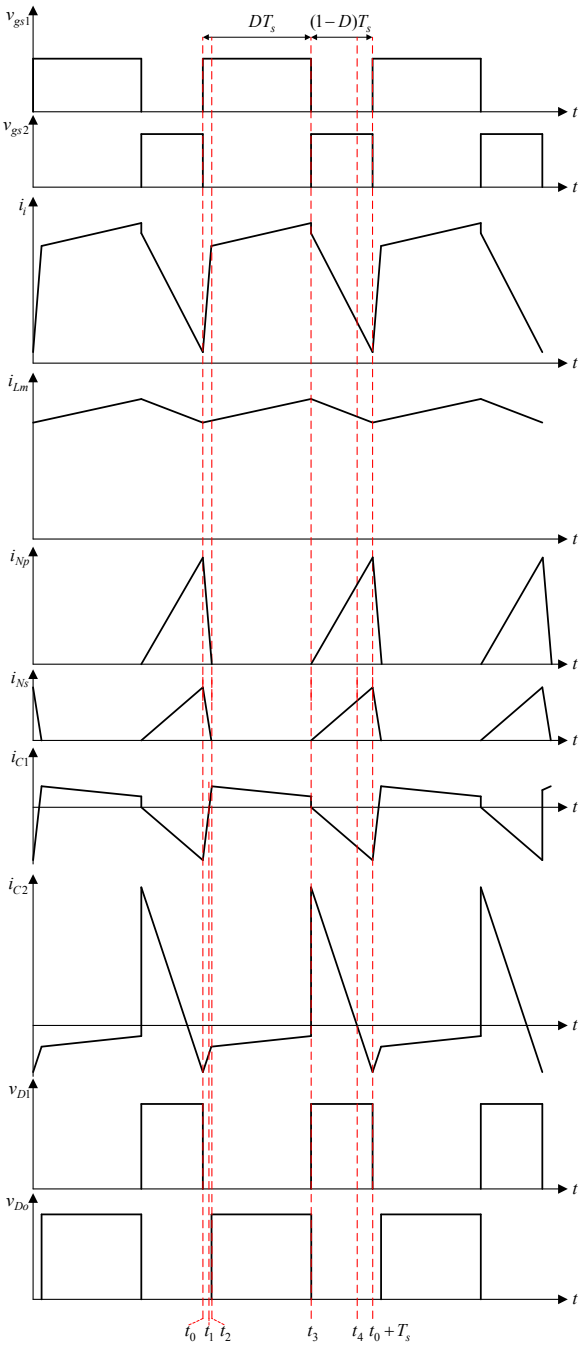

Fig. 7 Illustrated waveforms relevant to the proposed converter operating.

State 1: $[\, t_0 \le t \le t_1 \,]$

The switch S_1 is on and S_2 is off, the diode D_1 is on, and the output diode D_o is on, as shown in Fig. 8. At the same time, the energy required by the load is supplied by the input voltage V_i , the energy-transferring capacitors C_1 and C_2, and the energy stored in the leakage inductor L_{k2}. At the instant of t_1, the energy-transferring capacitor C_2 stops discharging, and state 1 ends.

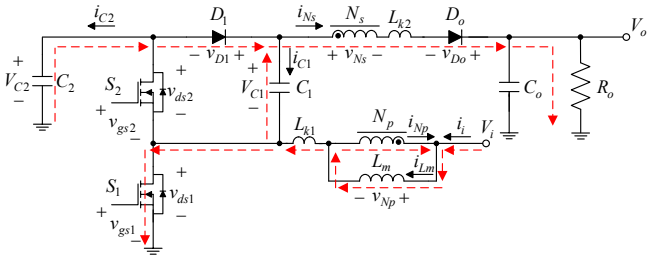

Fig. 8 Current flow of state 1.

State 2: $[\, t_1 \le t \le t_2 \,]$

The switch S_1 is on and the switch S_2 is off, the diode D_1 is on, and the output diode D_o is on, as shown in Fig. 11. At the same time, the energy-transferring capacitor C_2 charges the energy-transferring capacitor C_1, and, together with the energy stored in the leakage inductor L_{k2}, provides the energy for the load. At the instant of t_2, the current in the coupled inductor on the secondary side drops to zero, and state 2 ends.

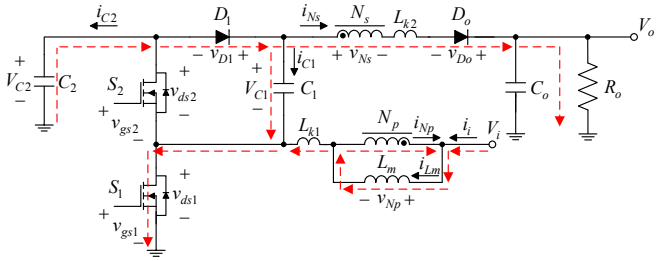

Fig. 9 Current flow of state 2.

State 3: $[\, t_2 \le t \le t_3 \,]$

The switch S_1 is on and the switch S_2 is off, the diode D_1 is on, and the output diode D_o is off, as shown in Fig. 10. At the same time, the voltage across the magnetizing inductor L_m and leakage inductor L_{k1} is the input voltage V_i, so both inductors are in the magnetization state. At the same time, the energy-transferring capacitor C_2 charges the energy-transferring capacitor C_1, and the output capacitor C_o provides the energy for the load. At the instant of t_3, the switch S_1 is turned off and the switch S_2 is turned on, and state 3 ends.

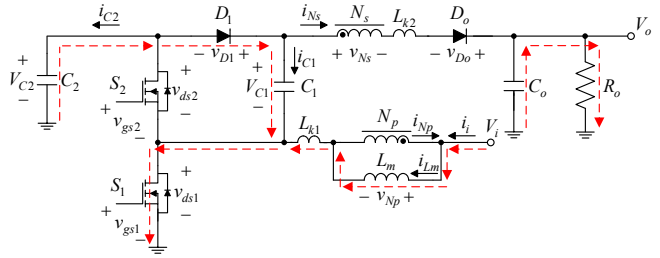

Fig. 10 Current flow of state 3.

State 4: $[\, t_3 \le t \le t_4 \,]$

The switch S_1 is off and the switch S_2 is on, the diode D_1 is off, and the output diode D_o is on, as shown in Fig. 11. At the same

time, the voltage across the magnetizing inductor L_m and leakage inductor L_{k1} is the input voltage V_i minus the voltage across the energy-transferring capacitor C_2, so both inductors are in the demagnetization state. In addition, the input voltage V_i, magnetizing inductor L_m and leakage inductor L_{k1} charge the energy-transferring capacitor C_2, and, together with the energy-transferring capacitor C_1, provide the energy for the load. At the instant of t_4, the energy-transferring capacitor C_2 stops charging, and state 4 ends.

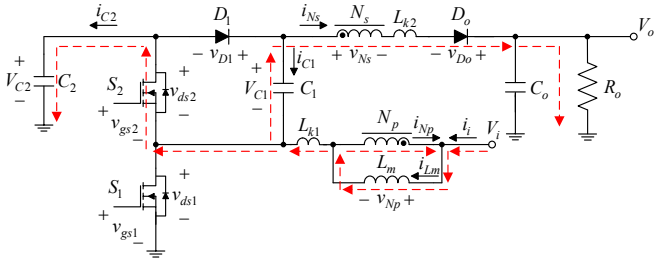

Fig. 11 Current flow of state 4.

State 5: $[\, t_4 \le t \le t_0 + T_s \,]$

The switch S_1 is off and the switch S_2 is on, the diode D_1 is off and the output diode D_o is on, as shown in Fig. 12. At the same time, in addition to the path of energy supply to the load as described in state 4, the energy-transferring capacitor C_2 also supplies energy to the load. At the instant of t_0+T_s, the switch S_1 is turned on and the switch S_2 is turned off, and state 5 ends and returns to state 1, completing one cycle.

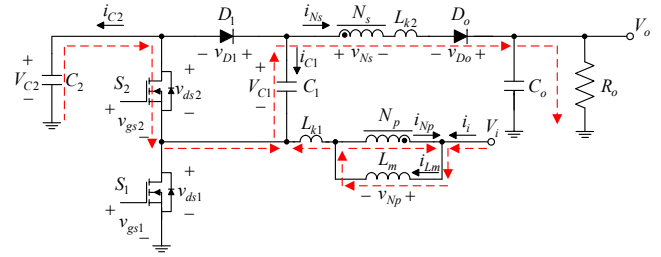

Fig. 12 Current flow of state 5.

To simplify the analysis, the voltage conversion ratio of the proposed structure will not consider the leakage inductances, so state 1 and state 2 can be ignored.

The equations corresponding to state 3 can be found in Fig. 10 as

$$\begin{cases} v_{Np} = V_i \\ V_{C2} = V_{C1} \end{cases} \tag{19}$$

From Figs. 11 and 12, the equations corresponding to states 4 and 5 are

$$\begin{cases} v_{Np} = V_i - V_{C2} \\ v_{Np} = V_i + V_{C1} - v_{Ns} - V_o \end{cases} \tag{20}$$

where

$$\begin{cases} v_{Ns} = v_{Np} \times n \\ V_{C1} = V_{C2} \end{cases} \tag{21}$$

Substituting (21) into (20), (20) can be rewritten as

$$\begin{cases} v_{Np} = V_i - V_{C1} \\ v_{Np} = \dfrac{V_i + V_{C1} - V_o}{1+n} \end{cases} \tag{22}$$

The voltage across the magnetizing inductor Lm must obey the volt-second balance in the steady state to obtain

$$V_i D + (V_i - V_{C1})(1-D) = 0 \tag{23}$$

$$V_i D + (\frac{V_i + V_{C1} - V_o}{1+n})(1-D) = 0 \tag{24}$$

Rearranging (23) yields

$$\frac{V_{C1}}{V_i} = \frac{1}{1-D} \tag{25}$$

Then, substituting (25) into (24) yields

$$\frac{V_o}{V_i} = \frac{2+nD}{1-D} \tag{26}$$

4. BOUNDARY CONDITION FOR THE MAGNETIZING INDUCTANCE

Assume that this converter has no loss in power conversion, i.e. $P_i = P_o$. Then, by using equation (26), we get

$$I_i = \frac{2+nD}{1-D} I_o \tag{27}$$

Also

$$I_o = \frac{V_o}{R_o} \tag{28}$$

Therefore, (27) can be rewritten as

$$I_i = \frac{2+nD}{1-D} \times \frac{V_o}{R_o} \tag{29}$$

The average value of the magnetizing inductance current is

$$I_{Lm} = I_i + I_{Np} \tag{30}$$

The average current of the primary winding I_{Np} is n times of the average current of the secondary winding I_{Ns}, where $n=N_s/N_p$, and the average current of the secondary winding I_{Ns} is equal to the output current I_o, i.e.,

$$\begin{cases} I_{Np} = nI_{Ns} \\ I_{Ns} = I_o \end{cases} \tag{31}$$

Thus, (30) can be rewritten as

$$I_{Lm} = I_i + nI_o \tag{32}$$

Finally, by substituting (28) and (29) into (32), we get

$$I_{Lm} = \frac{2+nD}{1-D} \times \frac{V_o}{R_o} + n\frac{V_o}{R_o} \tag{33}$$

By rearranging (33), we can obtain

$$I_{Lm} = \frac{2+n}{1-D} \times \frac{V_o}{R_o} \tag{34}$$

Since the current ripple flowing through the magnetizing inductor L_m, called Δi_{Lm}, can be expressed as

$$\Delta i_{Lm} = \frac{v_{Lm}\Delta t}{L_m} = \frac{V_i D T_s}{L_m} \tag{35}$$

Therefore, since the magnetizing inductor L_m will always operate in CCM, i.e.,

$$\begin{aligned} & 2I_{Lm} \geq \Delta i_{Lm} \\ \Rightarrow & \frac{2\times(2+n)}{1-D}\frac{V_o}{R_o} \geq \frac{V_i D T_s}{L_m} \\ \Rightarrow & \frac{2L_m}{R_o T_s} \geq \frac{(1-D)^2 D}{(2+n)(2+nD)} \\ \Rightarrow & K \geq K_{crit}(D) \end{aligned} \tag{36}$$

where $K = \frac{2L_m}{R_o T_s}$ 且 $K_{crit}(D) = \frac{(1-D)^2 D}{(2+n)(2+nD)}$ 。

From the equation (36), it can be seen as $K \geq K_{crit}(D)$, the magnetizing inductor L_m operates in CCM; otherwise, it operates in the discontinuous conduction mode (DCM). Therefore, Fig. 13 shows the boundary between the two modes.

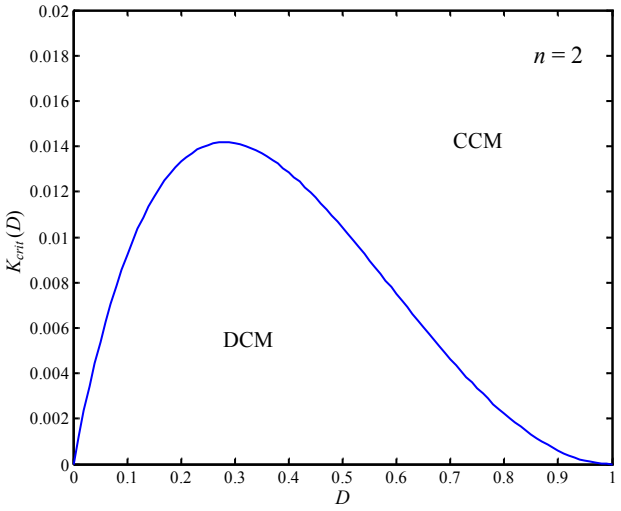

Fig. 13 Boundary between CCM and DCM.

5. SYSTEM SPECIFICATIONS AND COMPONENT SELECTION

Fig. 14 shows the system configuration of the proposed converter, consisting of the main power stage and the feedback control circuit. The main power stage is derived from the KY boost converter, and the feedback control circuit is composed of a voltage divider to obtain the analog signal of the output voltage, and an ADC to convert the analog signal into a digital signal. In addition, the gate drivers are used to drive the switches.

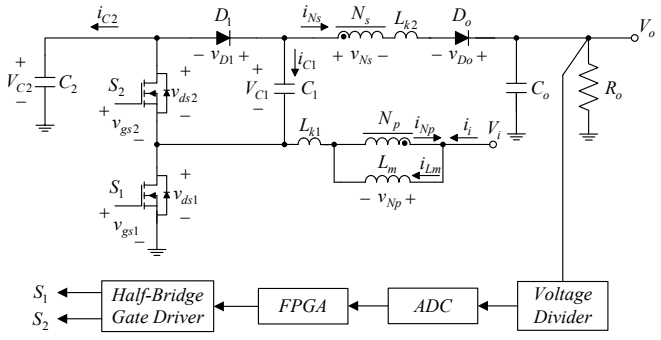

Fig. 14 System configuration of the proposed converter.

The system specifications are: (i) the input voltage is 20V; (ii) the output voltage is 200V; (iii) the rated output current is 1A and the minimum output current is 0.1A; (iv) the switching frequency 100kHz ; (v) the product names of the switches S_1 and S_2 are AP70T15GP-HF and STP120NF10, respectively; (vi) the product name of the diode D_1 is MUR860; (vii) the product name of the diode D_o is V20120C; (viii) the values of the energy-transferring capacitors C_1 and C_2 are 220μF (Rubycon) paralleled with 22μF (Rubycon) and 220μF (Rubycon) paralleled with 22μF (Rubycon); (ix) the value of the output capacitor is 100μF (Rubycon); and (x) FPGA adopts EP1C3T100C8N with 5136 logic elements, 423936 RAM bits, 23 multipliers, 2 PLLs, and 94 user I/O.

6. DESIGN OF TURNS RATIO AND DUTY CYCLE

Since the voltage conversion ratio of the conventional boost converter is theoretically infinite, but the components are parasitic components, resulting in a limited duty cycle, so the maximum operation is only about 0.6~0.7. By substituting the system specifications into (26) the range of turns ratio can be obtained to be

$$\begin{aligned} & 0.6 \le \frac{V_o - 2V_i}{nV_i + V_o} \le 0.7 \\ & \Rightarrow 0.6 \le \frac{200 - 2\times 20}{n\times 20 + 200} \le 0.7 \\ & \Rightarrow 1.43 \le n \le 3.33 \end{aligned} \tag{37}$$

For the convenience of winding the coupling inductor, the turns ratio is taken as an integer, i.e., the turns ratio can be 2 or 3, but since the turns ratio is proportional to the voltage stress on the diode D_o, the turns ratio is finally chosen to be

$$n = 2 \tag{38}$$

By substituting (38) and the system specifications into (26), we can get the duty cycle as

$$D = \frac{V_o - 2V_i}{nV_i + V_o} = \frac{200 - 2\times 20}{2\times 20 + 200} \cong 0.667 \tag{39}$$

Eventually, the magnetizing inductance L_m of the proposed circuit is designed by substituting the results of (38) and (39) into (36) to make sure that L_m operate in BCM at light load. So, the value of L_m is chosen to be 55.46μH with a PC44PQ32/30Z-12 core used.

7. SIMULATION RESULTS

The proposed high voltage-boosting converter is simulated under PSIM software by using the parameters obtained from Secs. V and VI to verify its feasibility.

Fig. 15 displays the simulation of the proposed high voltage-boosting converter, and the open-loop simulation is performed under the rated output power of 200W.

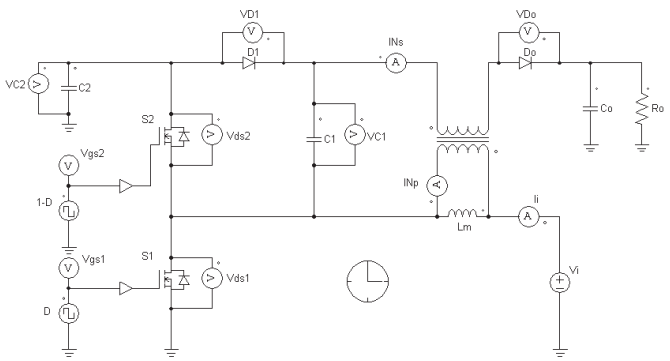

Fig. 15 Simulation circuit diagram.

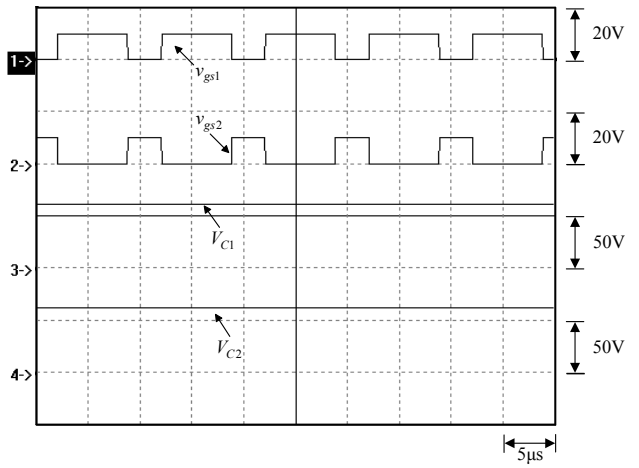

Fig. 16 Simulated waveforms at rated load:(1) v_{gs1} ; (2) v_{gs2} ; (3) V_{C1} ; (4) V_{C2} .

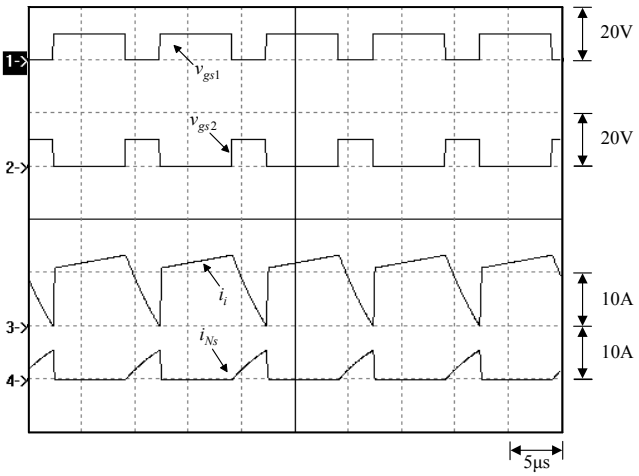

Fig. 17 Simulated waveforms at rated load:(1) v_{gs1} ; (2) v_{gs2} ; (3) i_i ; (4) i_{Ns} .

From Fig. 16, it can be seen the voltages on the energy-transferring capacitors can be stabilized at certain values, and from Fig. 17, the simulation results are almost consistent with the analysis results shown in Sec. III, so the feasibility of the proposed converter is verified.

8. EXPERIMENTAL RESULTS

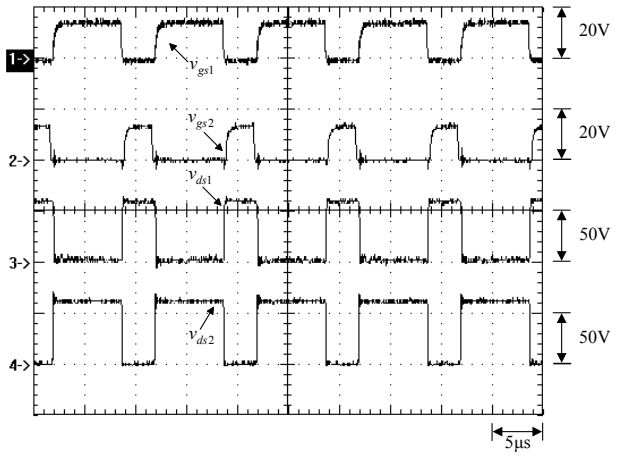

Fig. 18 Measured waveforms at light load:(1) v_{gs1}; (2) v_{gs2}; (3) v_{ds1}; (4) v_{ds2}.

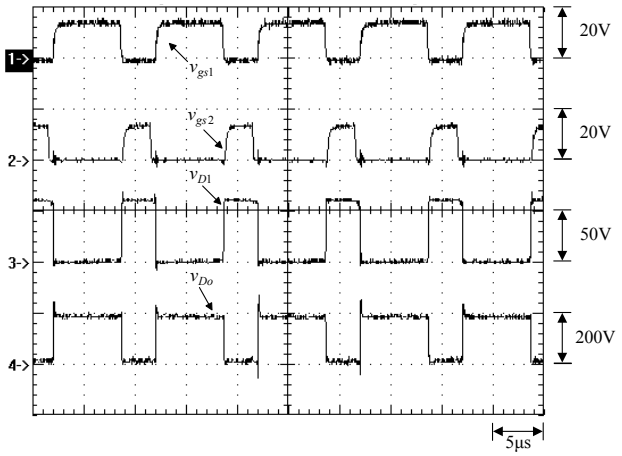

Fig. 19 Measured waveforms at light load:(1) v_{gs1}; (2) v_{gs2}; (3) v_{D1}; (4) v_{Do}.

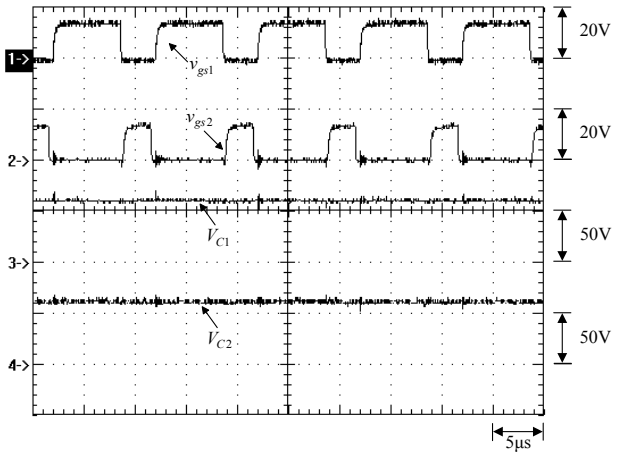

Fig. 20 Measured waveforms at light load:(1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

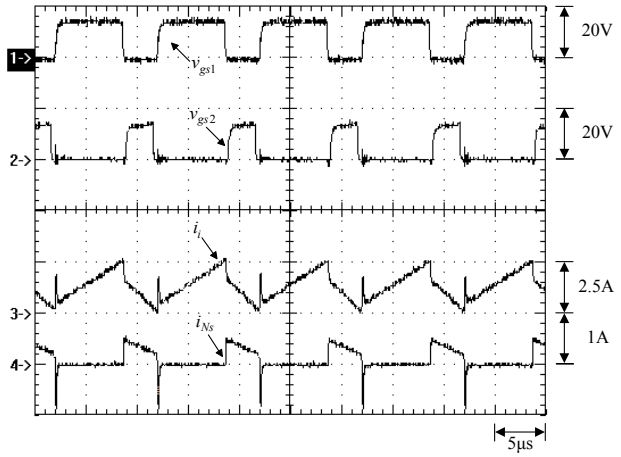

Fig. 21 Measured waveforms at light load:(1) v_{gs1}; (2) v_{gs2}; (3) i_i; (4) i_{Ns}.

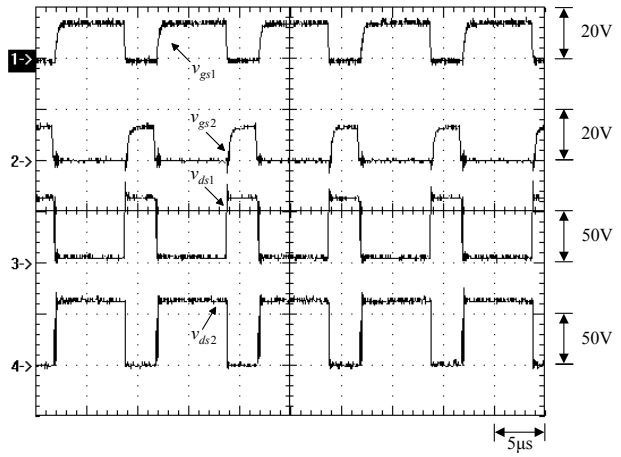

Fig. 22 Measured waveforms at half load:(1) v_{gs1}; (2) v_{gs2}; (3) v_{ds1}; (4) v_{ds2}.

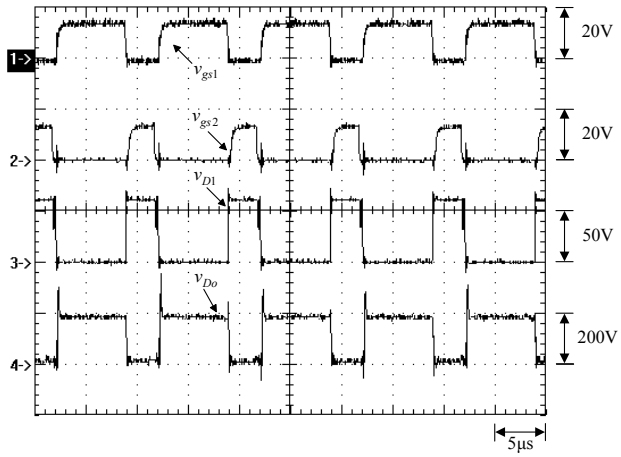

Fig. 23 Measured waveforms at half load:(1) v_{gs1}; (2) v_{gs2}; (3) v_{D1}; (4) v_{Do}.

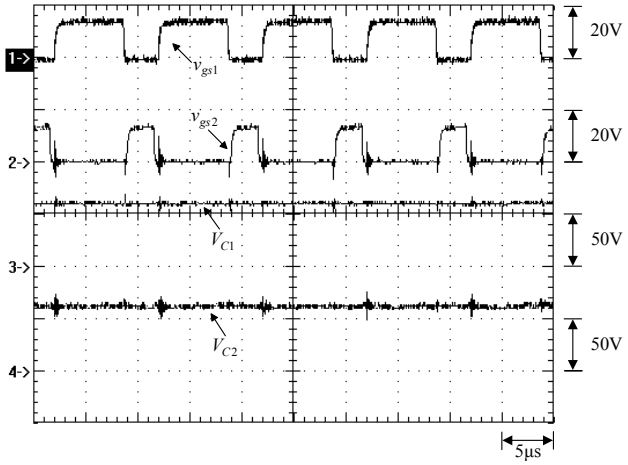

Fig. 24 Measured waveforms at half load:(1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

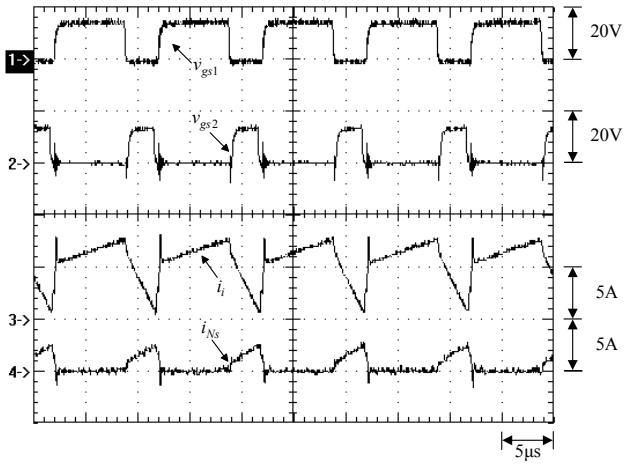

Fig. 25 Measured waveforms at half load:(1) v_{gs1}; (2) v_{gs2}; (3) i_i; (4) i_{Ns}.

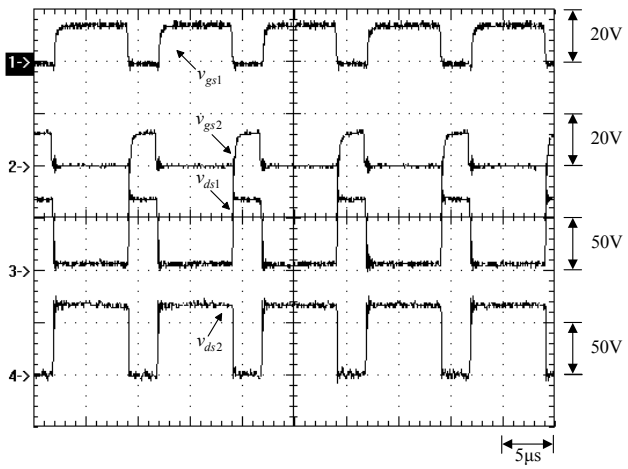

Fig. 26 Measured waveforms at rated load:(1) v_{gs1}; (2) v_{gs2}; (3) v_{ds1}; (4) v_{ds2}.

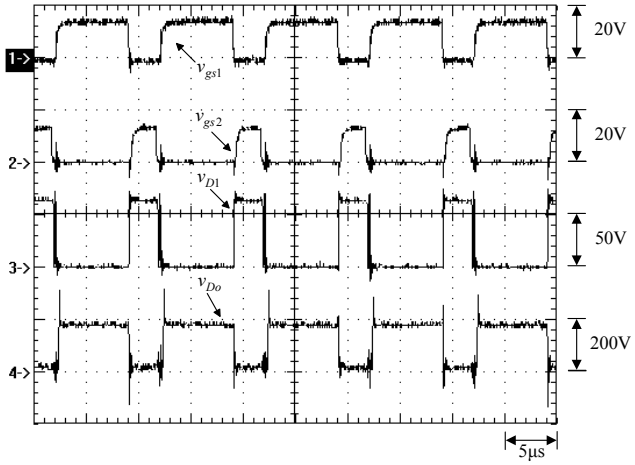

Fig. 27 Measured waveforms at rated load:(1) v_{gs1}; (2) v_{gs2}; (3) v_{D1}; (4) v_{Do}.

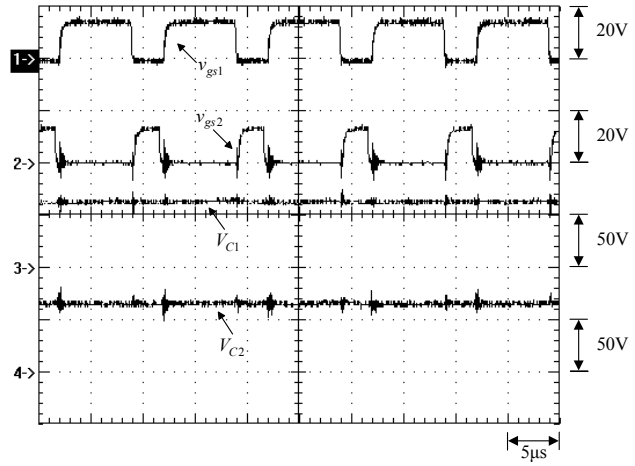

Fig. 28 Measured waveforms at rated load:(1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4) V_{C2}.

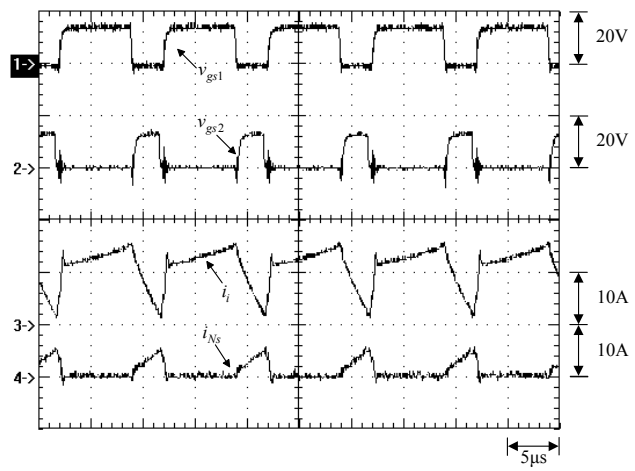

Fig. 29 Measured waveforms at rated load:(1) v_{gs1}; (2) v_{gs2}; (3) i_i; (4) i_{Ns}.

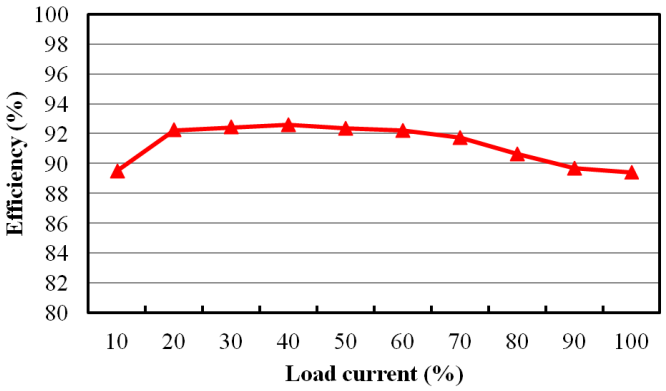

Fig. 30 Curve of efficiency versus load current.

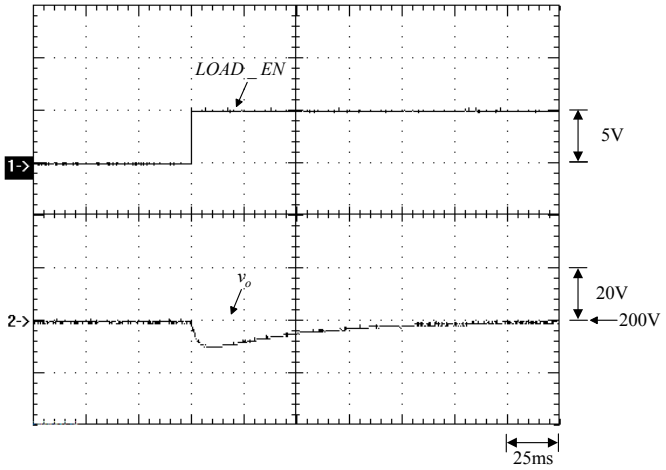

Fig. 31 Load transient response of the proposed converter from light load to half load.

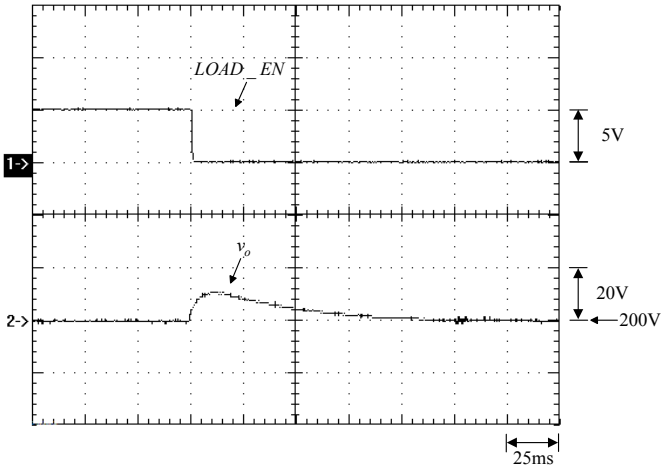

Fig. 32 Load transient response of the proposed converter from half load to light load.

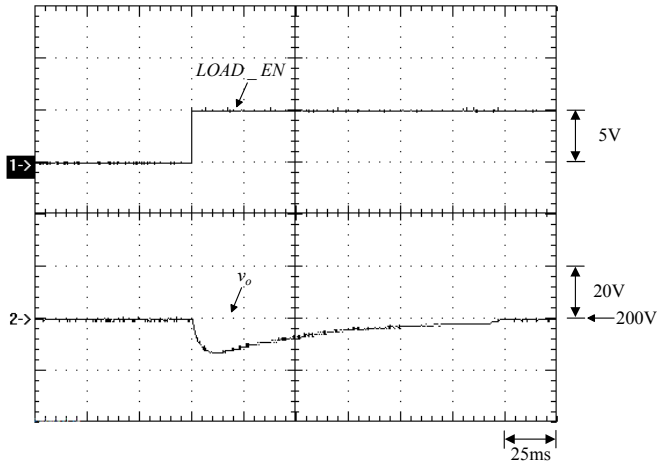

Fig. 33 Load transient response of the proposed converter from half load to rated load.

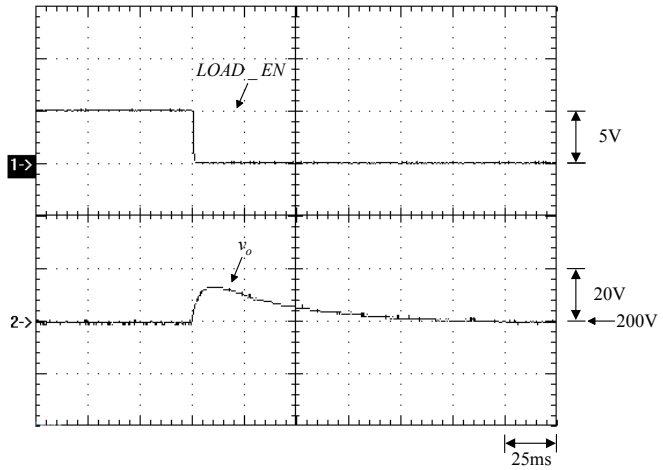

Fig. 34 Load transient response of the proposed converter from rated load to half load.

From Figs. 18, 19, 22, 23, 26 and 27, it can be seen the voltage spike of the switch S_1, the diode D_1 and the diode D_o will become larger with the increase of load. The ringing phenomenon of the diode D_o is caused by the resonance between the parasitic capacitance of the diode and the leakage inductance L_{k2} of the coupling inductor and the parasitic inductance on the line when the switch is turned on. Since the parasitic capacitance of the diode is not considered in the simulation, so this phenomenon does not occur. From Figs. 20, 24 and 28, it can be seen the voltages across the energy-transferring capacitors C_1 and C_2, called V_{C1} and V_{C2}, are stable at certain values for any load, and will increase slightly with the increase of load. From Figs. 21, 25 and 29, it can be seen the input current i_i and the secondary winding current i_{Ns} both increase with the increase of load, and the input current spike, when the switch is on, is caused by the reverse recovery current of the diode D_o. From Fig. 30, it can be seen the minimum efficiency of the proposed circuit can reach 89.4% at light load, and the maximum efficiency can reach 92.61% .

Fig. 31 and Fig. 32 show the response of output voltage when the load is loaded from light load to half load and unloaded from half load to light load, respectively. As can be seen from these two figures, the recovery time of the output voltage during the load change is about 110ms, and the change in the output voltage during the load change is about 5% of the output voltage. Fig. 33 and Fig. 34 display the response of the output voltage when the load is loaded from half load to full load and unloaded from full load to half load, respectively. As can be seen from these two figures, the recovery time of the output voltage during load change is about 125~150ms and the change in output voltage during load change is about 7% of the output voltage. From Figs. 31 to 34, it can be seen the load responses are stable to some extent.

9. CONCLUSION

In this paper, we propose a new high voltage-boosting converter with a modified KY boost converter that uses coupling inductors and charge-pump capacitors to achieve a higher voltage conversion ratio.

First, the feasibility of the proposed circuit is verified by using the PSIM simulation software, and finally use the field programmable logic gate array chip EP1C3T100C8N produced by Altera Corporation as the system control kernel to demonstrate the effectiveness of the proposed circuit. The results show that the efficiency of the proposed circuit can be above 89.4% for any load, and up to 92.61%.

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